IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG.PHILIPS LCD CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION; AU OPTRONICS CORPORATION; AU OPTRONICS CORPORATION AMERICA; TATUNG COMPANY; TATUNG COMPANY OF AMERICA, INC.; AND VIEWSONIC CORPORATION, Defendants.	Civil Action No. 06-726-JJF DEMAND FOR TRIAL BY JURY

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT AGAINST DEFENDANT AU OPTRONICS CORPORATION

Plaintiff LG.Philips LCD Co., Ltd. ("LG.Philips") for its First Amended Complaint against Defendant AU Optronics Corporation, and for its Complaint against Defendants Chi Mei Optoelectronics Corporation; AU Optronics Corporation America; Tatung Company; Tatung Company of America, Inc.; and ViewSonic Corporation (collectively the "Defendants") for injunctive and declaratory relief and for damages, including treble or multiple damages, for patent infringement, states and alleges as follows:

NATURE OF THE ACTION

1. LG.Philips is the owner of United States Patent No. 5,019,002 ("the '002 Patent"), United States Patent No. 5,825,449 ("the '449 Patent"), and United States Patent No. 4,624,737 ("the '737 Patent") (collectively the "Patents-in-Suit").

2. AU Optronics Corporation claims to be the owner by assignment of United States Patent No. 6,976,781 ("the '781 Patent"), United States Patent No. 6,778,160 ("the '160 Patent"), and United States Patent No. 6,689,629 ("the '629 Patent") (collectively "the AUO Patents").

3. This is a civil action for the infringement of the Patents-in-Suit, including the willful infringement of the Patents-in-Suit by Defendants, and for a declaration of invalidity and non-infringement of the claims of the AUO Patents.

4. The technology at issue involves the design and manufacture of Liquid Crystal Display modules ("LCDs"), which are a type of flat panel display that are incorporated into at least LCD portable computers, LCD computer monitors, and LCD televisions.

THE PARTIES

5. Plaintiff LG.Philips is a corporation organized under the laws of the Republic of Korea, having a place of business located in Seoul, Korea.

6. Defendant Chi Mei Optoelectronics Corporation ("Chi Mei") is a Taiwanese corporation, having its principal place of business at 2F, No. 1, Chi-Yeh Road, Tainan Science Based Industrial Park, Hsinshih Hsiang, Tainan Hsien 710, TAIWAN 74147, R.O.C. Chi Mei manufactures LCD products in Taiwan and China and, on information and belief, directs those products to the United States, including Delaware, through established distribution channels involving various third parties, knowing that these third parties will use their respective nationwide contacts and distribution channels to import into, sell, offer for sale, and/or use these products in Delaware and elsewhere in the United States.

7. Defendant AU Optronics Corporation ("AUO") is a Taiwanese corporation, having its principal place of business at 1, Li-Hsin Rd., II, Science-Based Industrial Park,

Hsinchu City 30077 Taiwan, ROC. AUO manufactures LCD products in Taiwan and China and, on information and belief, directs those products to the United States, including Delaware, through established distribution channels involving various third parties, knowing that these third parties will use their respective nationwide contacts and distribution channels to import into, sell, offer for sale, and/or use these products in Delaware and elsewhere in the United States.

8. Defendant AU Optronics Corporation America a/k/a AU Optronics America, Inc. ("AUO America") is a domestic subsidiary of AUO that either directly or indirectly imports into, sells, and/or offers for sale its products in Delaware and elsewhere in the United States. AUO America is a California corporation, having its principal place of business at 1800 Wyatt Drive, Suite 7, Santa Clara, CA 95054. AUO America markets and sells AUO's products throughout the United States.

9. Defendant Tatung Company ("Tatung") is a Taiwanese corporation, having a place of business at 22 Chungshan N Rd. Section 3, Taipei, Taiwan. Tatung assembles LCD products in Taiwan and, on information and belief, directs those products to the United States, including Delaware, through established distribution channels involving various third parties, knowing that these third parties will use their respective nationwide contacts and distribution channels to import into, sell, offer for sale, and/or use these products in Delaware and elsewhere in the United States.

10. Defendant Tatung Company of America, Inc. ("Tatung America") is a domestic subsidiary of Tatung that either directly or indirectly imports into, sells, and/or offers for sale its products in Delaware and elsewhere in the United States. Tatung America is a California corporation, having a place of business at 2850 El Presidio Street, Long Beach, California 90810. Tatung America markets and sells Tatung's products throughout the United States.

11. Defendant ViewSonic Corporation ("ViewSonic") is a Delaware Corporation, having a place of business at 381 Brea Canyon Road, Walnut, California 91789, which either directly or indirectly imports into, sells, and/or offers for sale its products in Delaware and elsewhere in the United States,

JURISDICTION AND VENUE

12. This action is based upon and arises under the Patent Laws of the United States, 35 U.S.C. § 100 *et seq.*, and in particular §§ 271, 281, 283, 284 and 285, and is intended to redress infringement of the Patents-in-Suit owned by LG.Philips.

13. Additionally, this action is under the Declaratory Judgment Act, 28 U.S.C. §§ 2201 and 2202, and the Patent Laws of the United States, based upon an actual controversy between LG.Philips and AUO regarding the validity and infringement of the claims of the AUO Patents, and is intended to provide appropriate and necessary declaratory relief.

14. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

15. Defendants have transacted and continue to transact business in the United States and in this judicial district by: using or causing to be used; making; importing or causing to be imported; offering to sell or causing to be offered for sale; and/or selling or causing to be sold directly, through intermediaries and/or as an intermediary, a variety of products that infringe the Patents-in-Suit to customers in the United States, including customers in this judicial district, and Defendants will continue to do so unless enjoined by this Court.

16. This Court has personal jurisdiction over Chi Mei, AUO, and Tatung, and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c) and (d), and 28 U.S.C. § 1400(b), in that these Defendants are committing and are causing acts of patent infringement

within the United States and within this judicial district, including the infringing acts alleged herein, both directly, through one or more intermediaries, and as an intermediary, and in that these Defendants have caused and cause injury and damages in this judicial district by acts or omissions outside of this judicial district, including but not limited to utilization of their own distribution channels established in the United States and AUO America's and Tatung America's distribution channels in the United States, as set forth below, to ship a variety of products that infringe the Patents-in-Suit into the United States and into this judicial district while deriving substantial revenue from services or things used or consumed within this judicial district, and will continue to do so unless enjoined by this Court.

17. This Court has personal jurisdiction over AUO America and Tatung America and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c), and 28 U.S.C. § 1400(b), in that these Defendants are committing acts of patent infringement within the United States and within this judicial district, including the infringing acts alleged herein, both directly, through one or more intermediaries, and as an intermediary. AUO America and Tatung America regularly import large quantities of AUO, and Tatung LCD products into the United States for distribution throughout the United States, including in this judicial district. AUO America and Tatung America are involved in the distribution of infringing LCD products and are aware that their products are sold throughout the United States, including in Delaware. The established distribution networks of these Defendants consist of national distributors and resellers, and these Defendants distribute to national retailers that have stores located in Delaware. By shipping into, offering to sell in, using, or selling products that infringe the Patents-in-Suit in this judicial district, or by inducing or causing those acts to occur, AUO America and Tatung America have transacted and transact business and perform works and services in this judicial district, have

contracted and contract to supply services and things in this judicial district, have caused and cause injury and damages in this judicial district by acts and omissions in this judicial district, and have caused and cause injury and damages in this judicial district by acts or omissions outside of this judicial district while deriving substantial revenue from services or things used or consumed within this judicial district, and will continue to do so unless enjoined by this Court.

18. This Court has personal jurisdiction over ViewSonic, and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c), and 28 U.S.C. § 1400(b), in that ViewSonic is incorporated and therefore resides in Delaware for purposes of establishing venue in this district, in that ViewSonic has been doing business in Delaware, including the infringing acts alleged herein, both directly, through one or more intermediaries, and/or as an intermediary, and will continue to do so unless enjoined by this Court.

THE PATENTS-IN-SUIT

19. On May 28, 1991, the '002 Patent, entitled "Method of Manufacturing Flat Panel Backplanes including Electrostatic Discharge Prevention and Displays Made Thereby," was duly and legally issued. LG.Philips is the owner by assignment of all rights, title, and interest in and to the '002 Patent. A copy of the '002 Patent is attached as Exhibit A.

20. On October 20, 1998, the '449 Patent, entitled "Liquid Crystal Display Device and Method of Manufacturing the Same," was duly and legally issued. LG.Philips is the owner by assignment of all rights, title, and interest in and to the '449 Patent. A copy of the '449 Patent is attached as Exhibit B.

21. On November 25, 1986, the '737 Patent, entitled "Process for Producing Thin-Film Transistor," was duly and legally issued. LG.Philips is the owner by assignment of all

rights, title, and interest in and to the '737 Patent. A copy of the '737 Patent is attached as Exhibit C.

22. LG.Philips owns the Patents-in-Suit and possesses the right to sue and to recover for infringement of the Patents-in-Suit.

23. Defendants have been and are infringing and/or inducing infringement of the Patents-in-Suit because they at least use, cause to be used, make, import, cause to be imported, offer for sale, cause to be offered for sale, sell, and/or cause to be sold in this judicial district and elsewhere in the United States products that infringe the Patents-in-Suit.

FACTUAL BACKGROUND

24. LG.Philips has invested substantial time and money in designing, developing, manufacturing and producing LCD products that incorporate the patented LCD technology.

25. LG.Philips derives substantial benefits from the exploitation of its patented technology in the United States and abroad. LG.Philips' interests, including, but not limited to, these benefits have been and continue to be harmed by the Defendants' infringement of the Patents-in-Suit.

26. The Defendants at least use, cause to be used, make, import, cause to be imported, offer for sale, cause to be offered for sale, sell, and/or cause to be sold in the United States and in this judicial district LCDs and/or LCD products that are encompassed by and/or made by the methods claimed in the Patents-in-Suit.

27. The Defendants have induced and/or continue to induce the infringement of the Patents-in-Suit in the United States and in this judicial district.

28. Defendants maintain and develop relationships with business partners, including, for example, suppliers and customers, to promote and encourage the import, offering for sale, sale and use of its infringing visual display products in the United States.

29. Defendants actively sell to and solicit business from customers and distributors located in the United States. Defendants coordinate with these and other third parties concerning the designs, specifications, distribution and/or placement of orders regarding such LCDs and LCD products destined for the U.S. market.

30. Defendants also communicate with third parties to promote and encourage the use, sale, importation and/or offering for sale of these same LCDs and LCD products in and into the United States.

31. Defendants have relationships with third parties to develop and supply the U.S. market with such LCDs and LCD products.

32. Defendants communicate and meet with third parties about their LCDs and LCD products and these communications and meetings facilitate the sale, offer for sale and/or distribution of Defendants' LCDs and LCD products to customers and users in the United States.

COUNT I
INFRINGEMENT OF THE '002 PATENT

33. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

34. Defendants have infringed, and/or induced infringement of the '002 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that are made by a method that

infringes one or more claims of the '002 Patent in this judicial district and elsewhere in the United States.

35. The products made by the infringing method that are used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by Defendants meet each and every limitation of at least one claim of the '002 Patent, either literally or equivalently.

36. LG.Philips has been and will continue to be injured by Defendants' past and continuing infringement of the '002 Patent and is without adequate remedy at law.

37. Defendants have, upon information and belief, infringed and are infringing the '002 Patent with knowledge of LG.Philips' patent rights and without a reasonable basis for believing their conduct is lawful. Defendants' infringement has been and continues to be willful and deliberate, and will continue unless enjoined by this Court, making this an exceptional case and entitling LG.Philips to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNT II
INFRINGEMENT OF THE '449 PATENT

38. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

39. Defendants have infringed and/or induced infringement of the '449 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that are made by a method that infringes one or more claims of the '449 Patent in this judicial district and elsewhere in the United States.

40. The products made by the infringing method that are used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by Defendants meet each and every limitation of at least one claim of the '449 Patent, either literally or equivalently.

41. LG.Philips has been and will continue to be injured by Defendants' past and continuing infringement of the '449 Patent and is without adequate remedy at law.

42. Defendants have, upon information and belief, infringed and are infringing the '449 Patent with knowledge of LG.Philips' patent rights and without a reasonable basis for believing their conduct is lawful. Defendants' infringement has been and continues to be willful and deliberate, and will continue unless enjoined by this Court, making this an exceptional case and entitling LG.Philips to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNT III
INFRINGEMENT OF THE '737 PATENT

43. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

44. Defendants have infringed and/or induced infringement of the '737 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that were made by a method that infringed one or more claims of the '737 Patent in this judicial district and elsewhere in the United States.

45. The products made by the infringed method that were used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to

be imported by Defendants meet each and every limitation of at least one claim of the '737 Patent, either literally or equivalently.

46. LG.Philips has been injured by Defendants' infringement of the '737 Patent.

47. Defendants have, upon information and belief, infringed the '737 Patent with knowledge of LG.Philips' patent rights and without a reasonable basis for believing their conduct was lawful. Defendants' infringement has been willful and deliberate, making this an exceptional case and entitling LG.Philips to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNT IV
CLAIM FOR DECLARATORY JUDGMENT OF INVALIDITY OF THE '781 PATENT, THE '160 PATENT, AND THE '629 PATENT AGAINST DEFENDANT AU OPTRONICS CORPORATION

48. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

49. AUO has accused LG.Philips of infringing AUO's United States Patent No. 6,976,781 (the "'781 Patent")(a copy of which is attached as Exhibit D), United States Patent No. 6,778,160 (the "'160 Patent")(a copy of which is attached as Exhibit E), and United States Patent No. 6,689,629 (the "'629 Patent")(a copy of which is attached as Exhibit F) by filing a complaint in the U.S. District Court for the Western District of Wisconsin. As such, there is a substantial controversy between the parties having adverse legal interests.

50. Claims of the '781 Patent are invalid for failure to satisfy one or more of the requirements for patentability set forth in Title 35 of the United States Code.

51. Claims of the '160 Patent are invalid for failure to satisfy one or more of the requirements for patentability set forth in Title 35 of the United States Code.

52. Claims of the '629 Patent are invalid for failure to satisfy one or more of the requirements for patentability set forth in Title 35 of the United States Code.

53. Because AUO has asserted the AUO Patents against LG.Philips, thereby creating an actual controversy, declaratory relief is both appropriate and necessary to establish that one or more of the claims of the '781 Patent, the '160 Patent, and the '629 Patent are invalid.

COUNT V
CLAIM FOR DECLARATORY JUDGMENT OF NON-INFRINGEMENT OF THE '781 PATENT, THE '160 PATENT, AND THE '629 PATENT AGAINST DEFENDANT AU OPTRONICS CORPORATION

54. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

55. LG.Philips' LCD modules do not infringe any claim of the '781 Patent, either directly or under the doctrine of equivalents.

56. LG.Philips' LCD modules and/or methods of driving LCD modules do not infringe any claim of the '160 Patent, either directly or under the doctrine of equivalents.

57. LG.Philips' LCD modules and/or methods for forming LCD modules do not infringe any claim of the '629 Patent, either directly or under the doctrine of equivalents.

58. Because AUO maintains that LG.Philips infringes the AUO Patents, thereby creating an actual controversy, a declaration of rights between LG.Philips and AUO is both appropriate and necessary to establish that LG.Philips has not infringed and does not infringe any claim of the '781 Patent, the '160 Patent, or the '629 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff LG.Philips prays for judgment as follows:

A. That Chi Mei, AUO, AUO America, Tatung, Tatung America, and ViewSonic have infringed the Patents-in-Suit;

B. That Chi Mei's, AUO's, AUO America's, Tatung's, Tatung America's, and ViewSonic's infringement of the Patents-in-Suit has been willful;

C. That Chi Mei, AUO, AUO America, Tatung, Tatung America, and ViewSonic and their parents, subsidiaries, affiliates, successors, predecessors, assigns, and the officers, directors, agents, servants and employees of each of the foregoing, and those persons acting in concert or participation with any of them, are enjoined and restrained from continued infringement, including but not limited to using, making, importing, offering for sale and/or selling products that infringe, and from inducing the infringement of, the '002 Patent and '449 Patent, prior to their expiration, including any extensions;

D. That Chi Mei, AUO, AUO America, Tatung, Tatung America, and ViewSonic and their parents, subsidiaries, affiliates, successors, predecessors, assigns, and the officers, directors, agents, servants and employees of each of the foregoing, and those persons acting in concert or participation with any of them deliver to LG.Philips all products that infringe the Patents-in-Suit for destruction at LG.Philips' option;

E. That a judgment be entered against AUO declaring that the claims of United States Patent No. 6,976,781, United States Patent No. 6,778,160, and United States Patent No. 6,689,629 are each invalid, and thus unenforceable against LG.Philips, its officers, agents, servants and employees;

F. That a judgment be entered against AUO declaring that LG.Philips has not infringed and does not infringe any claim of United States Patent No. 6,976,781, United States Patent No. 6,778,160, and United States Patent No. 6,689,629;

G. That LG.Philips be awarded monetary relief adequate to compensate LG.Philips for Chi Mei's, AUO's, AUO America's, Tatung's, Tatung America's, and ViewSonic's acts of

infringement of the Patents-in-Suit within the United States prior to the expiration of the Patents-in-Suit, including any extensions;

H. That any monetary relief awarded to LG.Philips regarding the infringement of the Patents-in-Suit by Defendants be trebled due to the willful nature of Chi Mei's, AUO's, AUO America's, Tatung's, Tatung America's, and ViewSonic's infringement of the Patents-in-Suit;

I. That any monetary relief awarded to LG.Philips be awarded with prejudgment interest;

J. That this is an exceptional case and that LG.Philips be awarded the attorneys' fees, costs and expenses that it incurs prosecuting this action; and

K. That LG.Philips be awarded such other and further relief as this Court deems just and proper.

JURY DEMAND

Plaintiff demands a trial by jury of any and all issues triable of right by a jury.

April 11, 2007

THE BAYARD FIRM

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EXHIBIT A

United States Patent [19]

Holmberg

[11] **Patent Number: 5,019,002**

[45] **Date of Patent: May 28, 1991**

[54] **METHOD OF MANUFACTURING FLAT PANEL BACKPLANES INCLUDING ELECTROSTATIC DISCHARGE PREVENTION AND DISPLAYS MADE THEREBY**

[75] Inventor: **Scott H. Holmberg**, San Ramon, Calif.

[73] Assignee: **Honeywell, Inc.**, Minneapolis, Minn.

[21] Appl. No.: **218,312**

[22] Filed: **Jul. 12, 1988**

[51] **Int. Cl.**[5] **H01L 45/00**

[52] **U.S. Cl.** **445/24**; 357/23.13; 437/56

[58] **Field of Search** 445/24, 3; 357/23.13, 357/4; 437/4, 8, 56

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,455,739	6/1984	Hynecek	427/8 X
4,586,242	5/1986	Harrison	437/8
4,714,949	12/1987	Simmons et al.	357/23.13
4,736,271	4/1988	Mack et al.	357/23.13
4,803,536	2/1989	Tuan	357/23.13

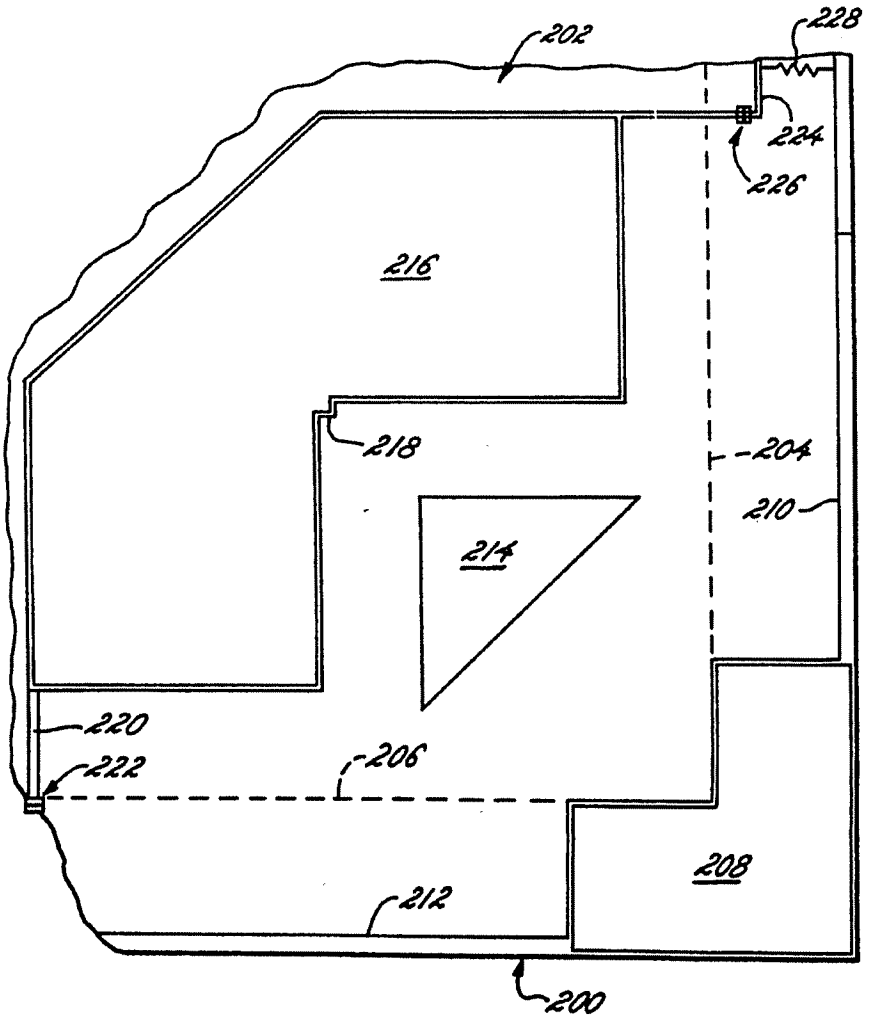
Primary Examiner—Kenneth J. Ramsey

Attorney, Agent, or Firm—Leydig, Voit & Mayer

[57] **ABSTRACT**

Flat panel displays are provided including protection from electrostatic discharge (ESD) during manufacture and thereafter. At least one ESD guard ring is provided to protect the active elements of the display from the potential discharge between the row and column lines. An internal ESD guard ring is coupled to the row and column lines via shunt transistors. An external ESD guard ring is coupled to the row and column lines via a resistance. Both of the guard rings can be provided; however, the external guard ring is removed prior to completion of the display.

36 Claims, 5 Drawing Sheets



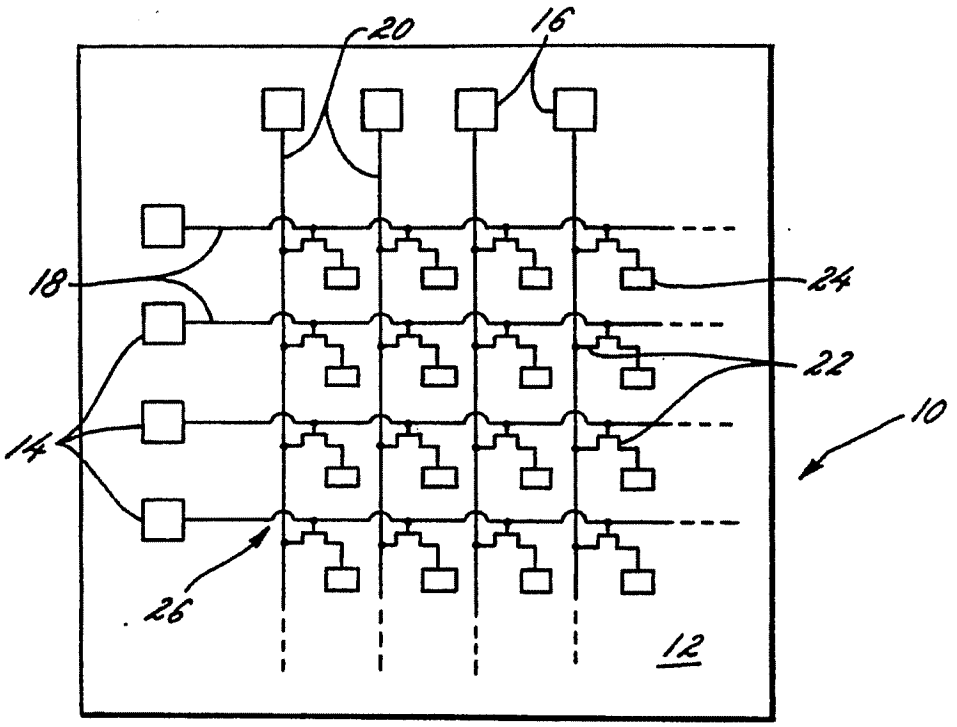


FIG. 1

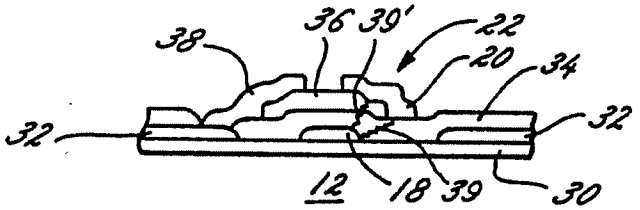
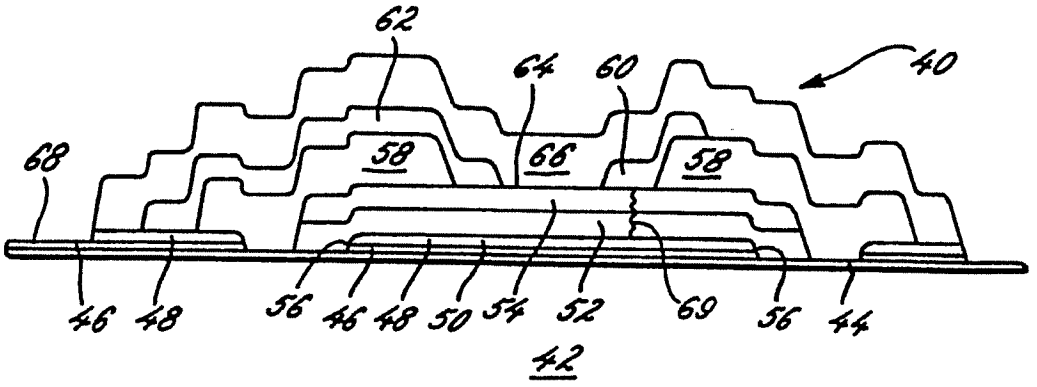


FIG. 2

FIG. 3



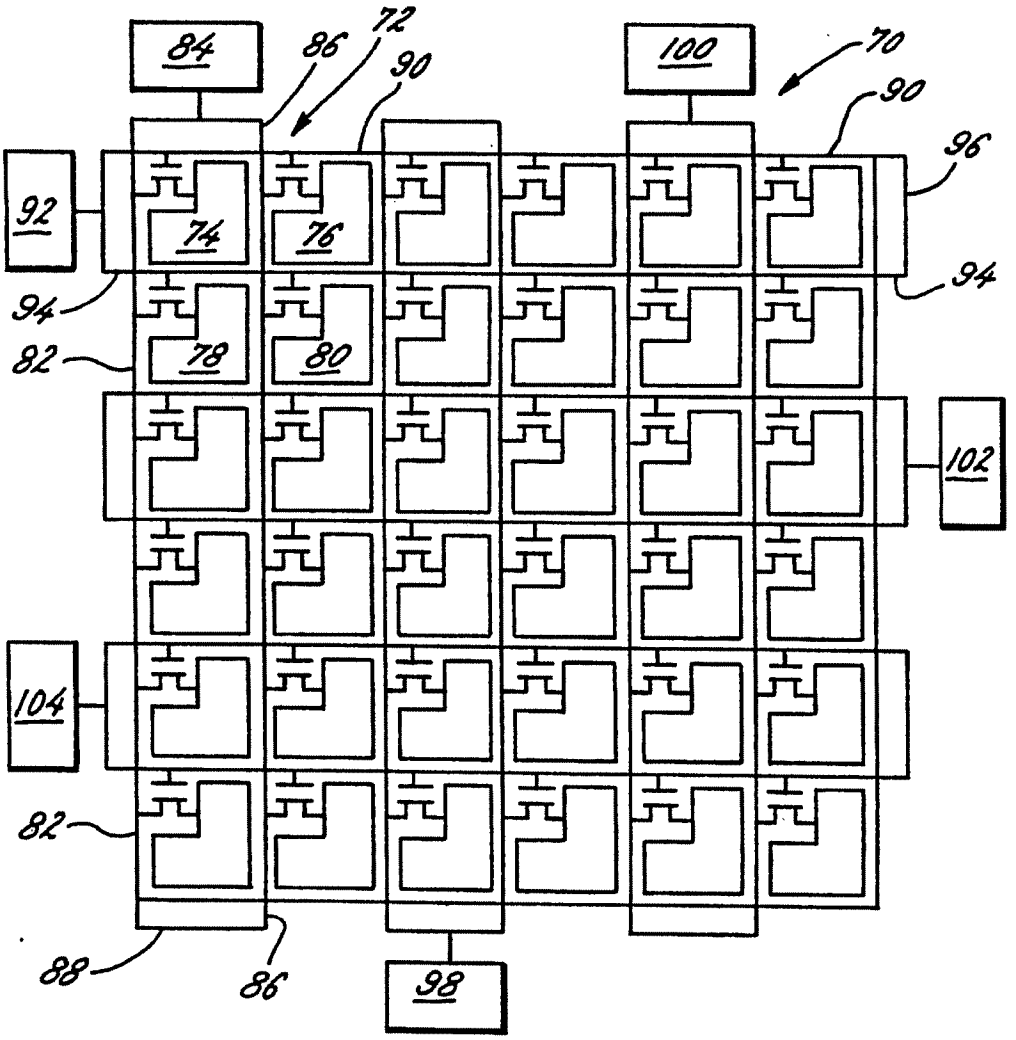
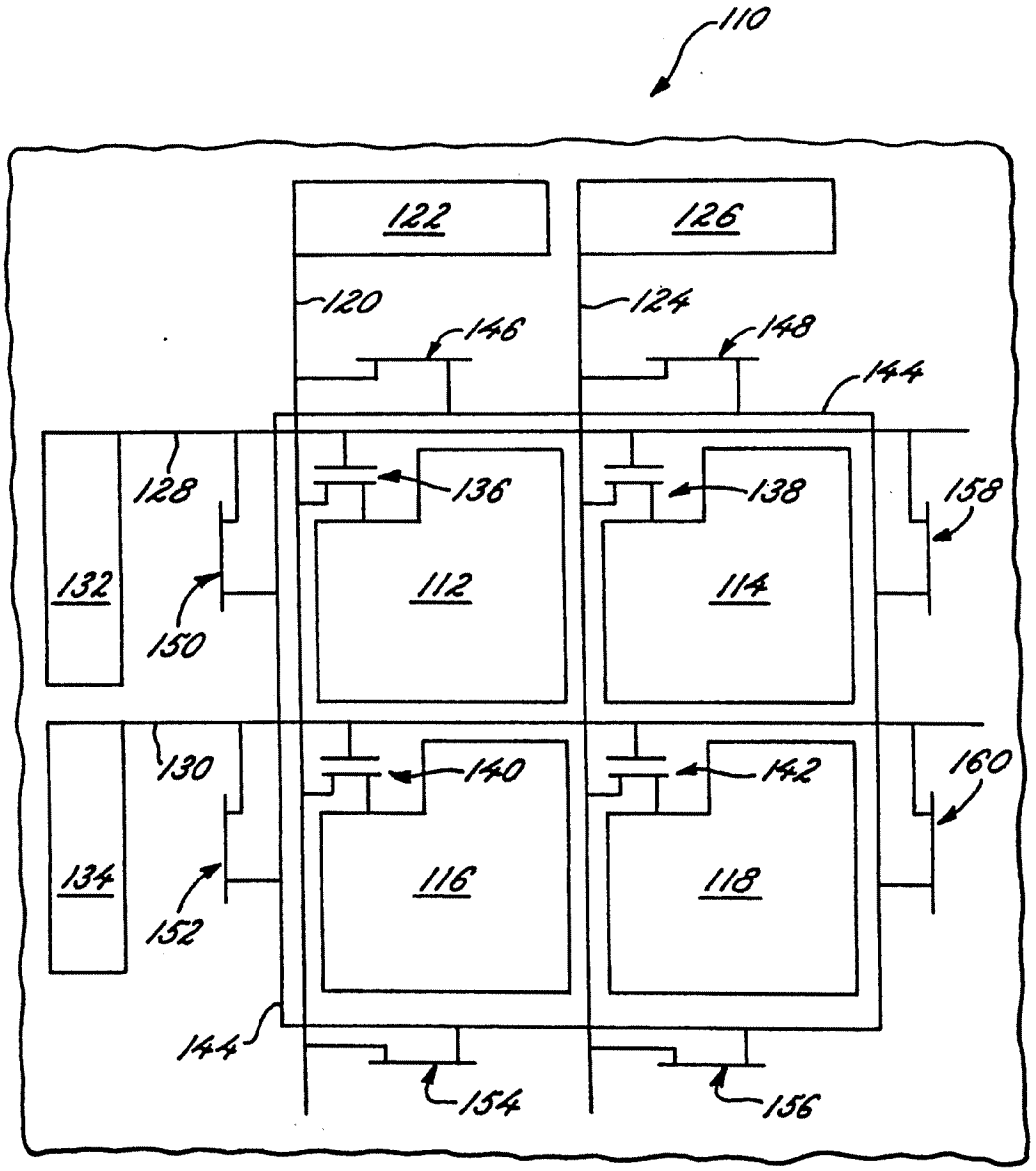


FIG. 4

FIG. 5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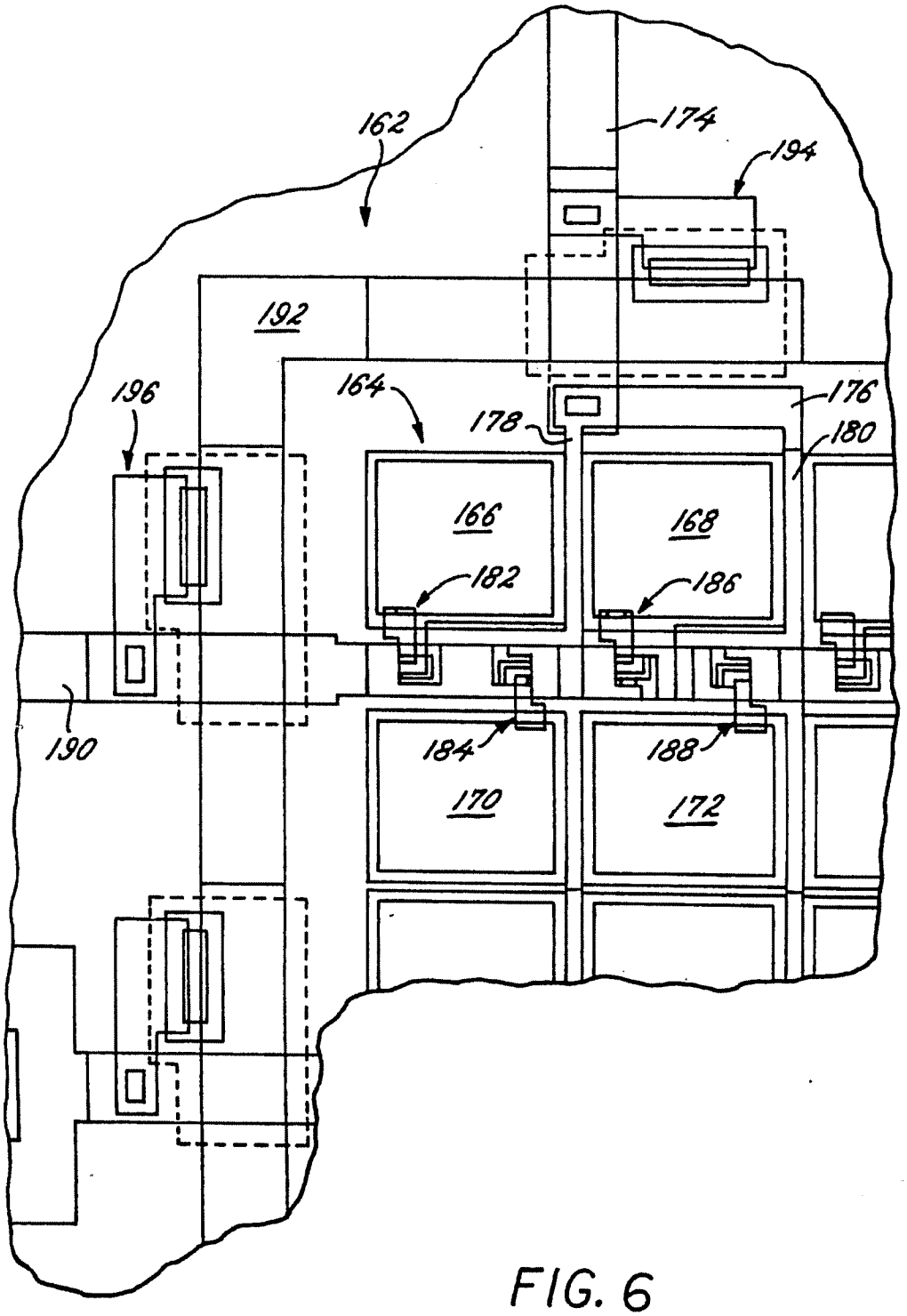
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FIG. 6

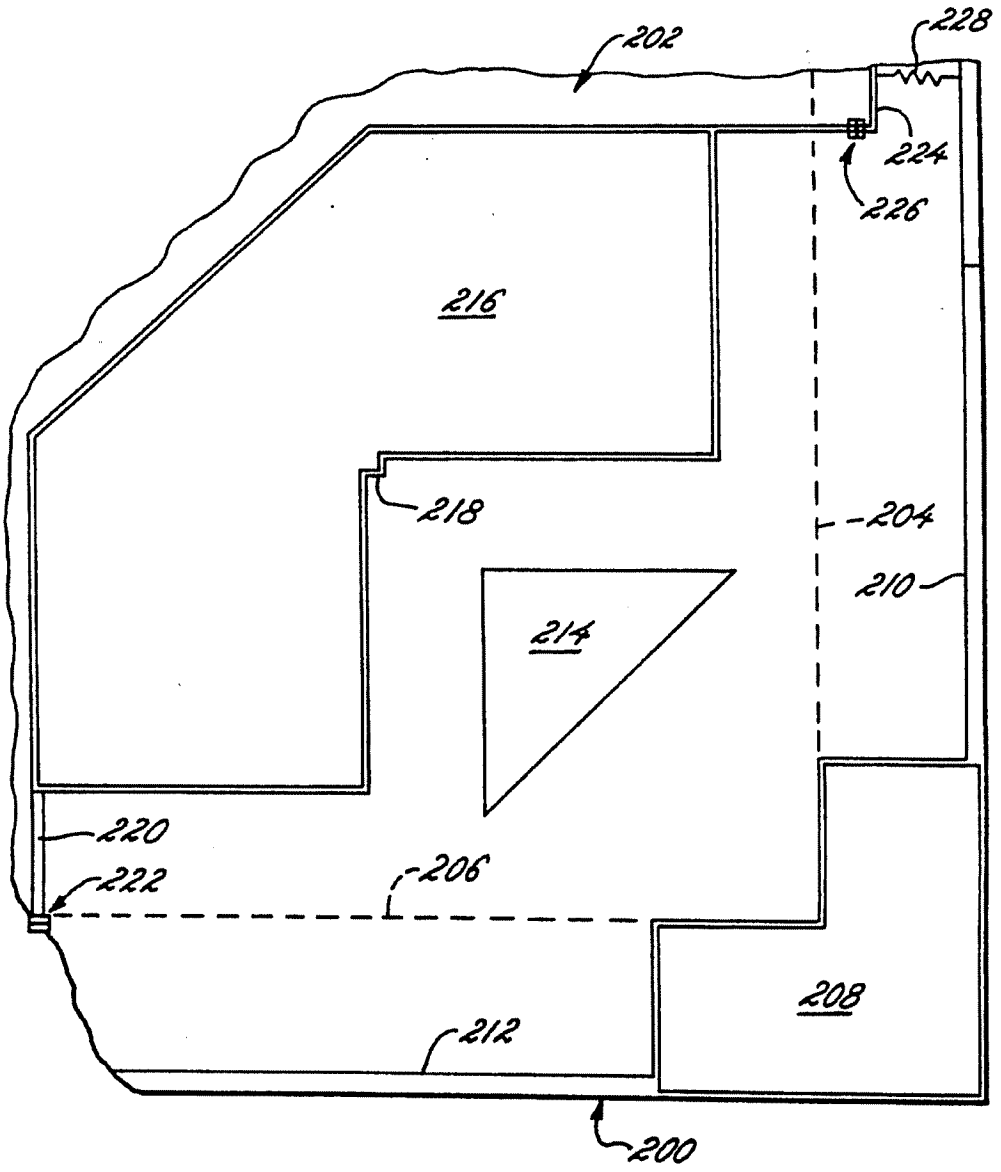

FIG. 7

METHOD OF MANUFACTURING FLAT PANEL BACKPLANES INCLUDING ELECTROSTATIC DISCHARGE PREVENTION AND DISPLAYS MADE THEREBY

BACKGROUND OF THE INVENTION

The present invention pertains to improved flat panel displays and methods of making the displays with protection from electrostatic discharges. More particularly, the present invention is directed to methods of increasing the manufacturing yields of flat panel display backplanes and the displays made therefrom by improving handling characteristics.

In recent years there has been growing interest in flat panel displays, such as those which employ liquid crystals, electrochromic or electroluminescence, as replacements for conventional cathode ray tubes (CRT). The flat panel displays promise lighter weight, less bulk and substantially lower power consumption than CRT's. Also, as a consequence of their mode of operation, CRT's nearly always suffer from some distortion. The CRT functions by projecting an electron beam onto a phosphor-coated screen. The beam will cause the spot on which it is focused to glow with an intensity proportional to the intensity of the beam. The display is created by the constantly moving beam causing different spots on the screen to glow with different intensities. Because the electron beam travels a further distance from its stationary source to the edge of the screen than it does to the middle, the beam strikes various points on the screen at different angles with resulting variation in spot size and shape (i.e. distortion).

Flat panel displays are manufactured to be substantially free of such distortion. In the manufacture of flat panel displays the circuit elements are deposited and patterned, generally by photolithography, on a substrate, such as glass. The elements are deposited and etched in stages to build a device having a matrix of perpendicular rows and columns of circuit control lines with a pixel contact and control element between the control line rows and columns. The pixel contact has a medium thereon which is a substance that either glows (active) or changes its response to ambient light (passive) when a threshold voltage is applied across the medium control element. The medium can be a liquid crystal, electroluminescent or electrochromic materials such as zinc sulfide, a gas plasma of, for example, neon and argon, a dichroic dye, or such other appropriate material or device as will luminesce or otherwise change optical properties in response to the application of voltage thereto. Light is generated or other optical changes occur in the medium in response to the proper voltage applied thereto. Each optically active medium is generally referred to as a picture element or "pixel".

The circuitry for a flat panel display is generally designed such that the flat panel timeshares, or multiplexes, digital circuits to feed signals to one row and column control line of the pixels at a time. Generally one driving circuit is used for each row or column control line. In this way a subthreshold voltage can be fed to an entire row containing hundreds of thousands of pixels, keeping them all dark or inactive. Then a small additional voltage can be supplied selectively to particular columns to cause selected pixels to light up or change optical properties. The pixels can be made to glow brighter by applying a larger voltage or current of a longer pulse of voltage or current. Utilizing liquid crystal displays (LCD's) with twisted nematic active material, the display is substantially transparent when not activated and becomes light absorbing when activated. Thus, the image is created on the display by sequentially activating the pixels, row by row, across the display. The geometric distortion described above with respect to CRT's is not a factor in flat panel displays since each pixel sees essentially the same voltage or current.

One of the major problems that arises with respect to the prior art method of manufacture of backplanes for active matrix displays (e.g. those employing thin film transistors at each pixel) is that they generally suffer production yield problems similar to those of integrated circuits. That is, the yields of backplanes produced are generally not 100% and the yield (percentage of backplanes with no defects) can be 0% in a worst case. High quality displays will not tolerate any defective pixel transistors or other components. Also, larger size displays are generally more desirable than smaller size displays. Thus, a manufacturer is faced with the dilemma of preferring to manufacture larger displays, but having to discard the entire product if even one pixel is defective. In other words, the manufacturer suffers a radically increased manufacturing cost per unit resulting from decreasing usable product yield.

One solution to the low yield problem is disclosed in U.S. Ser. No. 948,224, filed Dec. 31, 1986, now U.S. Pat. No. 4,676,761 entitled "Method of Manufacturing Flat Panel Backplanes Including Improved Testing and Yields Thereof and Displays Made Thereby", which is owned by the assignee of the present application and is incorporated herein by reference.

These problems of increased cost and decreased yield are improved in the present invention by providing methods of manufacturing display backplanes and the resulting displays with electrostatic discharge protection which provide protection against fatal defects during and after manufacture of the displays.

SUMMARY OF THE INVENTION

There is provided improved methods of manufacturing backplanes and the resulting flat panel displays to increase the manufacturing yield, decrease manufacturing costs and substantially eliminate fatal display defects caused by electrostatic discharge during manufacture and thereafter.

These improvements are accomplished by forming at least one electrostatic discharge (ESD) guard ring around the active elements of the display. An internal ESD guard ring can be formed, which provides a discharge path for static potential applied across the row and column line of the display. This prevents the potential from discharging between the row and column lines through an active element causing a short and resulting in a defect in the display during manufacture or thereafter. An external ESD guard ring can be formed, which provides protection during manufacture of the displays, however, the external ESD guard ring is removed at the end of the display manufacturing process. The displays also can include both the internal and external ESD guard ring to provide protection during manufacture and thereafter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view schematic representation of an active matrix display backplane made by a prior art method;

FIG. 2 is a cross-section of one transistor of the prior art backplane which could be utilized with the present invention;

FIG. 3 is a cross-section of one transistor which could be utilized with the present invention;

FIG. 4 is a plan view schematic representation of one prior embodiment of a subpixel matrix display;

FIG. 5 is a plan view schematic representation of a matrix display illustrating one embodiment of an internal ESD guard ring of the present invention;

FIG. 6 is an enlarged plan view of a portion of one embodiment of a subpixel matrix display illustrating the internal ESD guard ring in accordance with the present invention; and

FIG. 7 is a partial plan view of one embodiment of an exterior ESD guard ring of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to FIG. 1, there is shown a schematic representation of an active matrix flat panel display device 10 made in accordance with conventional photolithographic techniques. One such device 10 and the manufacture thereof is more fully described in Application of Amorphous Silicon Field Effect Transistors in Addressable Liquid Crystal Display Panels, A. J. Snell, et al., *Applied Physics*, No. 24, p. 357, 1981. The device 10 includes a substrate 12, sets of contact pads 14 and 16, sets of control or bus lines 18 and 20, and, in this particular example of the prior art, transistors 22 and pixel back contacts 24.

The substrate 12 commonly employed in these devices is formed from glass. The control lines 18 and 20 are organized into a matrix of rows 18 and columns 20. The control line rows 18 in this device 10 serve as gate electrodes and the control line columns 20 as source connections. One contact pad 14 is connected to one end of each of the row control lines 18. One contact pad 16 is connected to one end of each of the column control lines 20. The display drive control (not shown) is connected to the sets of pads 14 and 16.

At each matrix crossover point 26, where a row line 18 and a column line 20 cross, a switching element, transistor 22 is formed to connect the row line 18 and column line 20 to the pixel back contacts 24. The active medium is deposited at least on the contacts 24 which will optically change properties in response to the combined voltages or currents in the respective crossover point 26 formed by the row 18 and column 20. The active medium at a given crossover point 26 will appear as a square or dot in the overall checkerboard type matrix of the display 10. The actual size of the transistors 22 and the contacts 24 are not now drawn to scale, but are shown schematically for illustration only.

It should be noted that theoretically there is no limit on the number of rows 18 and columns 20 that can be employed, only a portion of which are illustrated in FIG. 1. Therefore, there is also no theoretical limit on the outside dimensions of such a device 10. However, the present state of the lithographic art places a practical limit on the outside dimensions of these devices. The present alignment techniques generally allow high resolution display devices to be manufactured approximately five inches on a side 28, although improved techniques of up to fourteen inches on a side has been demonstrated.

The problem encountered by the prior art method of manufacture is that if the array of device 10 contains any defective pixel transistors 22 or other circuit elements causing a pixel to be inoperative, it must be discarded.

Referring in detail to FIG. 2, several problems occur when the switching element, transistor 22 is manufactured. The substrate 12 is a substantial portion of the backplane cost and hence an inexpensive soda-lime glass is generally utilized. It has been demonstrated by liquid crystal display manufacturers that the high sodium concentration can poison the liquid crystal materially diffusing through the overlying ITO layer and hence an SiO_2 suppression layer 30 is generally formed on the substrate 12. There are some high quality low sodium types of substrates available, which would not need the suppression layer 30. An ITO layer 32 is formed and etched to provide an ITO free area on which the gate 18 is deposited. Following the deposition of the gate 18, a gate insulator layer 34 is deposited. Although a smooth uniform coverage of the gate 18 by the insulator 34 is illustrated, in production the gate 18 has or can have sharp edges which lead to pin holes or thinning of the insulator 34 at the gate edges. The source and drain metals can short to the gate 18. The thinning or pin holes produce transistors 22, which if operative, do not have uniform operating characteristics and hence the backplane is worthless.

One attempt to solve this problem, is to make the gate 18 very thin, but the resistivity is then too high to make the large arrays necessary for the backplane. A second attempt to solve the problem, is to make the gate insulator 34 very thick, but this decreases the gain of the transistor 22 and is also self defeating.

An amorphous silicon layer 36 is then deposited, with the source 20 and a drain 38 deposited thereover. A passivating layer (not shown) would be deposited over the completed structure to complete the transistor 22. During operation the activation of the source 20 and the gate 18 couples power through the silicon alloy 36 to the drain and hence to the contact pad 24 formed by the ITO layer 32.

During manufacture of the device 10, electrostatic discharge can occur when a high static electric potential is coupled across at least one pair of the gate lines 18 and the source lines 20. The discharge frequently will result in a short 39 through the insulator 34 or a short 39' through the insulator 34 and the silicon layer 36 in the transistor 22, between the adjacent crossover points of the lines 18 and 20 as can be seen in FIG. 2. This will cause at least one row and one intersecting column of the display pixels to be defective and in the type of display device 10, generally the defect will be a fatal one (clearly visible) and hence the device will be discarded. The device 10 does not provide any redundancy or subpixels and hence the defect cannot easily be isolated.

Referring now to FIG. 3, there is shown a schematic representation of one embodiment of a transistor 40 which can be utilized with the present invention. The transistor is more fully disclosed in U.S. Pat. Nos. 4,545,112 and 4,736,229, which are incorporated herein by reference.

A glass substrate 42 includes a barrier SiO_2 layer 44 thereon. As above mentioned, a low sodium glass sub-

strate, such as Corning 7059 glass, could be utilized, and hence the barrier layer **44** can be eliminated. The detailed deposition steps are described in the above-referenced patent and application. An ITO layer **46** is deposited and then a refractory metal layer **48** is deposited on the ITO layer **46**.

The layers **46** and **48** are etched to form a gate electrode **50**. A gate insulator **52** and a semiconductor material **54** are sequentially deposited over the gate **50**. The material **54** preferably is an amorphous silicon alloy. To avoid the possibility of any gate to source or drain shorts at gate edges **56**, a dielectric **58** is deposited over the gate **55**, the gate insulator **52** and the semiconductor **54**. The dielectric **58** is deposited to a sufficient thickness to ensure that no shorts or thin spots are formed between the edges **56** of the gate **50** and a source **60** and a drain **62** deposited thereover.

The dielectric **58** is etched away only on a substantially planar central region **64** of the semiconductor layer **54**. This insures uniform operating characteristics for the transistors **40** in the backplane array. A passivating layer **66** is deposited over the whole structure to complete the structure of the transistor **40**.

During all of the transistor processing steps, the refractory metal layer **48** remains over a pixel contact pad **68** upon which the active material of the pixel is deposited. As a final step, before the active medium (not shown) is added to the backplane to complete the display, the refractory metal is etched off of the pixel pad **68** leaving the ITO layer **46** exposed after all the processing has been completed.

The gate to source or drain shorts referred to above in discussing the dielectric **58**, refer to physical shorts caused by thin spots or actual metal particles or filaments. The electrostatic discharges caused during manufacturing and thereafter will be deterred by the dielectric **58**, but will not be eliminated. The potential can be high enough to again form a short **69** through the gate insulator **52** and the semiconductor material **54** in the transistor **40**, between the source **60** and the gate **50**. Depending upon the display structure, at least one pixel or one subpixel (FIG. **4**) will be defective.

Referring now to FIG. **4**, a subpixel matrix display of the above-referenced application, U.S. Ser. No. 948,224, is designated generally by the reference numeral **70**. The subpixel matrix display **70** is illustrated as having each pixel subdivided into four subpixels, but the pixels could be subdivided into numerous other configurations such as two subpixels, two by four or six subpixels or in three subpixels for color applications. Each pixel **72** is subdivided into four subpixels **74**, **76**, **78** and **30** (only one pixel **72** is so numbered for illustration). As previously stated, the number of pixels is merely shown for illustration purposes and the display **70** could contain any desired number and configuration, square or rectangular.

A column (source) line or bus **82** connects the subpixels **74** and **78** and all other column subpixel pairs in one-half of each of the pixels to a column or source contact pad **84** at one edge of the display **70**. A second column (source) line or bus **86** connects the subpixels **76** and **80** and all other column subpixel pairs in the second half of each of the pixels to the column or source contact pad **84**. The bus lines **82** and **86** are interconnected (shorted) at or before the pad **84** and are interconnected (shorted) at the opposite ends by a line or short **88**.

A row (gate) line or bus **90** connects the subpixels **74** and **76** and all other row subpixel pairs in one-half of each of the pixels to a row (gate) pad **92**. A second row (gate) line or bus **94** connects the subpixels **78** and **80** and all other row subpixel pairs in one-half of each of the pixels to the row pad **92**. The bus lines **90** and **94** are interconnected (shorted) at or before the pad **92** and are interconnected (shorted) at the opposite ends by a line or short **96**.

In a like manner, each of the other subpixel pairs are connected in columns to respective column (source) pads **98** and **100**, etc. The pads **84**, **98** and **100** are illustrated as being an opposite sides of the display to provide additional connecting space for the pads, however, they also could all be on one side as in the display **10**. Each of the other subpixel pairs also are connected in rows to respective row (gate) pads **102** and **104**, etc.

The pixel **72** then is divided into four subpixels **74**, **76**, **78** and **80** which allows for one of the subpixels to be defective, such as the subpixel **74**, without causing a fatal defect, since the remaining three subpixels **76**, **78** and **80** remain operative. In prior devices, the pixel **72** would be totally defective and hence the display **70** would be inoperable.

Further, one often fatal display defect is caused by a defect or open in one of the row or column bus lines which would cause the whole row or column to be out, again resulting in an inoperative display **70**. With the respective subpixels pairs of row and column bus lines interconnected, however, an open in a bus line will at most cause one subpixel to be inoperative. An open in one or more of the bus lines between the subpixels will result in no defects, since the current is supplied from the opposite shorted end of the row or column bus line. Thus, the display **70** in effect has redundant row and column bus lines.

To avoid the fatal defect of the multiple open lines, as also disclosed in U.S. Ser. No. 948,224, the redundant row and column bus lines can be further interconnected at each subpixel. Each pair of the column bus lines **82** and **86** are additionally interconnected between each of the subpixels **74**, **78**, etc. by respective lines or shorts. In a like manner, each pair of the row bus lines **90** and **94** are interconnected between each of the subpixels **74**, **76**, etc. by respective lines or shorts. Further, although both the row bus lines and the column bus lines can be interconnected between each subpixel, only one of the row or the column bus line sets might be shorted to limit the loss of active pixel display area.

The short **69** in one of the active devices in the display **70** can be eliminated by opening the row or column line between the short and the line. This results in only one subpixel, such as the subpixel **74** being defective and due to the small size of the subpixel, is not a fatal defect (i.e. not readily visual). The rest of the corresponding column and row subpixels would be operable due to the redundant and interconnected row and column bus lines.

Referring now to FIG. **5**, a matrix display incorporating one embodiment of an internal ESD guard ring of the present invention is designated generally by the reference numeral **110**. The matrix display **110** is illustrated having four pixels **112**, **114**, **116** and **118**. The pixels, however, can be subdivided into numerous subpixel configurations such as two or four subpixels, two by four or six subpixels or in three subpixels for color display applications. Also, as previously stated for the

subpixel matrix display **70**, the number of pixels can be of any number and configuration, square or rectangular.

A column (source) line or bus **120** connects the pixels **112** and **116** and all other pixels in the same column to a source contact pad **122** at one edge of the display **110**. A source line **124** connects the pixels **114** and **118** to a source contact pad **126**. In a like manner, a pair of row (gate) lines **128** and **130** connect respective pairs of pixels **112**, **114** and **116**, **118** in each row to respective gate pads **132** and **134**.

Each pixel **112**, **114**, **116** and **118** includes a respective active element, such as transistors **136**, **138**, **140** and **142** which couple the pixels to the respective source lines **120** or **124** and gate lines **128** or **130**. To prevent a large electrostatic potential discharging through one of the transistors **136**, **138**, **140** and **142**, an internal ESD guard ring **144** is formed around the pixels **112**, **114**, **116** and **118**. The guard ring **144** is illustrated as a closed ring, but could also be an open L or C-shaped line if the gate and source pads all are on one respective side of the display **110**.

The ESD guard ring **144** also is coupled via respective transistors **146**, **148**, **150** and **152** to, the source and gate lines. The guard ring **144** will be coupled to the end of each source and gate line, so if the source and gate lines include pads at their opposite ends (not illustrated), then the guard ring **144** will include a further respective set of transistors **154**, **156**, **158** and **160**.

The ESD guard ring **144** preferably is formed from a low resistance metal, such as an aluminum alloy. The transistors **146** through **160** can include a floating gate (not illustrated), no gate, or can include an oxide below to form a spark gap.

In operation, with the guard ring **144**, a potential placed upon the source pads **122** will not short one of the transistors **136** or **140**. Instead, the transistor **146** will turn on followed by the transistor **150**, shorting the potential from the pad **122**, via the line **120**, the transistor **146**, the guard ring **144**, the transistor **150** and the line **128** to the pad **132**. Thus, the guard ring **144** will not allow high potentials across the pads **122**, **126**, **132** and **134**. The guard ring **144** preferably is formed concurrently with the display elements and is not removed, providing continuous protection even following manufacture of the display **110**.

A specific subpixel display incorporating an internal guard ring of the invention is best illustrated in FIG. **6** and is designated generally by the reference numeral **162**. The display **162** includes a plurality of pixels, each having four subpixels in a similar fashion to the display **70** illustrated in FIG. **4**. Only one pixel **164** is illustrated in detail and includes four subpixels **166**, **168**, **170** and **172**. A source line **174** includes a shorting line **176** which is connected to a pair of source lines **178** and **180**, coupled to each of the subpixels by a respective transistor structure **182**, **184**, **186** and **188**, which are not described in detail. The transistors **182**, **184**, **186** and **188** also couple the subpixels **166**, **168**, **170** and **172** to a gate line **190**.

An internal ESD guard ring **192** is coupled via a transistor structure **194** to the source line **174** and via a transistor structure **196** to the gate line **190**. The guard ring **192** and transistors **194** and **196** operate as before described to short any potential to ground. The low value of the normal operating voltages does not turn on the transistors **194** and **196**, which do not effect the normal display operation.

The ESD preventive structure can also include an outer ESD guard ring **200**, best illustrated in FIG. **7**. Only one corner portion **202** of the display and guard ring **200** is illustrated. While the display is being manufactured, the outer guard ring **200** is connected to all of one of the source and gate pads (not illustrated), which pads are serially connected together via jumpers outside of scribe lines **204** and **206**. A corner pad **208** is connected to each other corner pad (not illustrated) by respective outer conductive lines **210** and **212** of the guard ring **200**. The L-shaped corner pad **208** can be grounded and also provides the alignment for the scribe lines **204** and **206**, which are utilized to disconnect the source and gate jumpers and the guard ring **200** after the structure is completed. The corner portion **202** includes a triangular pad **214** which provides alignment for diagonal corner displays, when utilized.

A backplane pickup contact pad **216** also is provided, which includes a corner **218** for aligning the backplane with the front plane. The pad **216** includes a shunt line **220** which is connected to one set of source or gate lines via a shunt transistor **222** along the edge to be scribed and removed along the line **206**. The line **210** is connected to the other set of gate or source lines by a shunt line **224**, a shunt transistor **226** and a large resistance **228**, such as 100 K ohms (illustrated schematically). The outer ESD guard ring **200** provides ESD protection only during manufacture of the display and is removed prior to completion of the display. The resistance **228** provides an ESD short for high electrostatic potentials, which can be incurred during manufacturing of the display which can be connected anywhere between the line **210** and the other set of gate or source lines. The resistance **228** minimizes the discharge current surge and the shunt transistors **222** and **226** act as before described. There will be at least one corner backplane pickup pad **216** and preferably there will be two or three, each with their associated shunt transistors.

The outer guard ring lines **210** and **212** preferably are formed at the same time as the firs: of the gate or source lines. The inner guard ring **44** and the associated shunt transistors of both guard rings preferably are formed concurrently with the other display structures. The scribe lines **204** and **206** can be prescribed, but left intact until the back and front planes are mated and then removed to provide the gate and source contacts for the printed circuit board connections.

Modification and variations of the present invention are possible in light of the above teachings. The transistors **22** or other types of two or three terminal switching devices can be utilized with the invention. The amorphous silicon alloy semiconductor material **54**, could be any of numerous types of materials such as CdSe or GaAs materials. The ESD guard rings can be utilized separately or together with all types of active element matrix displays and not just those illustrated. The shunt transistors **146**, **194** and **222**, etc. also can be formed as other active switching elements, such as diodes. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

What is claimed and desired to be secured by Letters Patent of the United States is:

1. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:

providing a substrate;

forming a pattern of pixels on said substrate;

forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;

forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

removing said outer guard ring and row and column interconnections prior to completion of the display.

2. The method as defined in claim **1** including coupling one plurality of said interconnected row and column lines to said outer guard ring via said resistance.

3. The method as defined in claim **2** including forming at least one pickup pad coupled to said resistance via a shunt switching element.

4. The method as defined in claim **3** including coupling said pickup pad to the other plurality of said interconnected row and column lines via another shunt switching element.

5. The method as defined in claim **3** including forming a corner on said pad to align the front plane and back plane of the display.

6. The method as defined in claim **3** including forming a plurality of pickup pads, each one on a separate corner of the display.

7. The method as defined in claim **1** including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections.

8. The method as defined in claim **1** including forming an inner electrostatic discharge guard ring on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

9. The method as defined in claim **8** including forming separate shunt switching elements between said inner guard ring and each row and column line.

10. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:

providing a substrate;

forming a pattern of pixels on said substrate;

forming a plurality of row and column intersecting pixel activation lines; and

forming an inner electrostatic discharge guard ring on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

11. The method as defined in claim **10** including forming separate shunt switching elements between said inner guard ring and each row and column line.

12. The method as defined in claim **10** including interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another and forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

removing said outer guard ring and row and column interconnections prior to completion of the display.

13. The method as defined in claim **12** including coupling one plurality of said interconnected row and column lines to said outer guard ring via said resistance.

14. The method as defined in claim **13** including forming at least one pickup pad coupled to said resistance via a shunt switching element.

15. The method as defined in claim **14** including coupling said pickup pad to the other plurality of said interconnected row and column lines via another shunt switching element.

16. The method as defined in claim **14** including forming a corner on said pad to align the front plane and back plane of the display.

17. The method as defined in claim **10** including forming a plurality of pickup pads, each one on a separate corner of the display.

18. The method as defined in claim **10** including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections.

19. An active matrix display backplane, comprising:

a substrate;

a pattern of pixels formed on said substrate;

a plurality of row and column intersecting pixel activation lines, substantially all of said row lines interconnected to one another and substantially all of said column lines interconnected to one another; and

an outer removable electrostatic discharge guard ring formed on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays.

20. The backplane as defined in claim **19** including one plurality of said interconnected row and column lines coupled to said outer guard ring via said resistance.

21. The backplane as defined in claim **20** including at least one pickup pad coupled to said resistance via a shunt switching element.

22. The backplane as defined in claim **21** including said pickup pad coupled to the other plurality of said interconnected row and column lines via another shunt switching element.

23. The backplane as defined in claim **21** including a corner formed on said pad to align the front plane and back plane of the display.

24. The backplane as defined in claim **21** including a plurality of pickup pads, each one formed on a separate corner of the display.

25. The backplane as defined in claim **19** including a corner pad formed on at least one corner of the display and having scribe lines aligned with said corner pad for removing said outer guard ring and row and column intersections.

26. The backplane as defined in claim **19** including an inner electrostatic discharge guard ring formed on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

27. The backplane as defined in claim **26** including separate shunt switching elements formed between said inner guard ring and each row and column line.

28. An active matrix display backplane, comprising:

a substrate;

a pattern of pixels formed on said substrate;

a plurality of row and column intersecting pixel activation lines; and

an inner electrostatic discharge guard ring formed on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

29. The backplane as defined in claim 28 including separate shunt switching elements formed between said inner guard ring and each row and column line.

30. The backplane as defined in claim 28 including substantially all of said row lines interconnected to one another and substantially all of said column lines interconnected to one another and an outer electrostatic discharge guard ring formed on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays.

31. The backplane as defined in claim 30 including one plurality of said interconnected row and column lines coupled to said outer guard ring via said resistance.

32. The backplane as defined in claim 31 including at least one pickup pad coupled to said resistance via a shunt switching element.

33. The backplane as defined in claim 32 including said pickup pad coupled to the other plurality of said interconnected row and column lines via another shunt switching element.

34. The backplane as defined in claim 32 including a corner formed on said pad to align the front plane and back plane of the display.

35. The backplane as defined in claim 28 including a plurality of pickup pads, each one formed on a separate corner of the display.

36. The backplane as defined in claim 28 including a corner pad formed on at least one corner of the display and having scribe lines aligned with said corner pad for removing said outer guard ring and row and column intersections.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,019,002

DATED : May 28, 1991

INVENTOR(S) : Scott H. Holmberg

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 2, lines 30-31, change "4,676,761" to --4,820,222--;

Col. 4, line 15, change "materially" to --material by--;

Col. 5, line 53, change "30" to --80--;
line 59, change "aIl" to --all--;

Col. 7, line 23, delete the third comma;

Col. 8, line 41, change "firs:" to --first--.

Signed and Sealed this

Twenty-third Day of February, 1993

Attest:

STEPHEN G. KUNIN

Attesting Officer

Acting Commissioner of Patents and Trademarks

EXHIBIT B

US005825449A

United States Patent [19]

Shin

[11] Patent Number: 5,825,449

[45] Date of Patent: Oct. 20, 1998

[54] **LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME**

[75] Inventor: **Woo Sup Shin**, Kyungsangbuk-do, Rep. of Korea

[73] Assignee: **LG Electronics, Inc.**, Seoul, Rep. of Korea

[21] Appl. No.: **781,188**

[22] Filed: **Jan. 10, 1997**

Related U.S. Application Data

[62] Division of Ser. No. 616,291, Mar. 15, 1996.

[30] **Foreign Application Priority Data**

Aug. 19, 1995 [KR] Rep. of Korea 25538/1995

[51] **Int. Cl.**[6] **G02F 1/136**; G02F 1/1343; G02F 1/1345

[52] **U.S. Cl.** **349/148**; 349/149; 349/43

[58] **Field of Search** 349/149, 148, 349/43, 139, 152, 147

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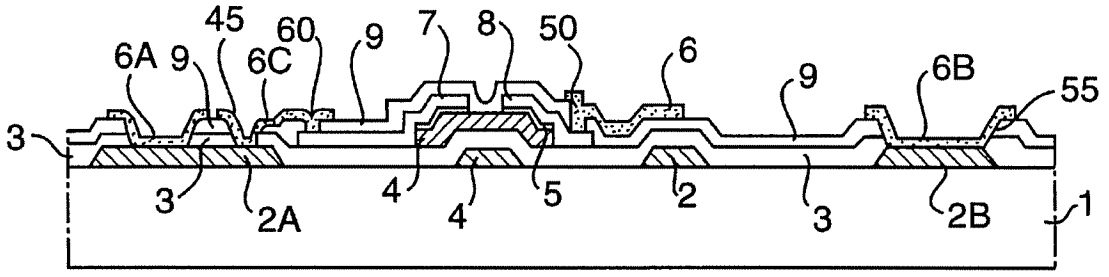
0 587 144	3/1994	European Pat. Off. .
0 620 473	10/1994	European Pat. Off. .

Primary Examiner—William L. Sikes
Assistant Examiner—Tiep H. Nguyen
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

[57] **ABSTRACT**

A method for fabricating a liquid crystal display is disclosed whereby a source and gate are exposed after the step of forming a passivation layer. As a result, the number of processing steps is reduced and yield is improved.

11 Claims, 5 Drawing Sheets



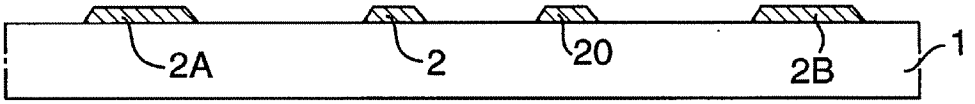


FIG. 1a
PRIOR ART

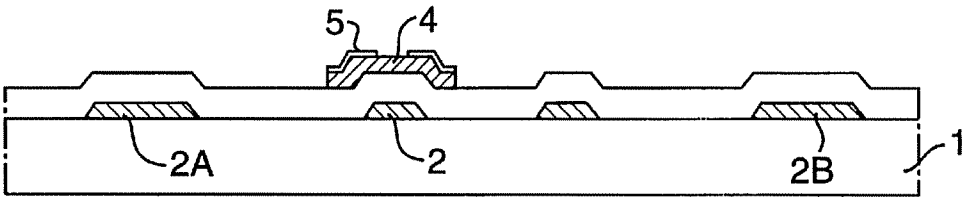


FIG. 1b
PRIOR ART

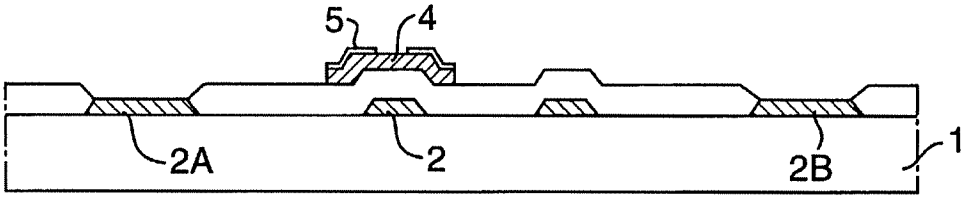


FIG. 1c
PRIOR ART

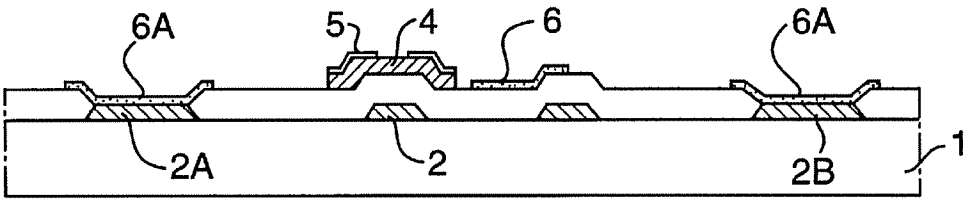


FIG. 1d
PRIOR ART

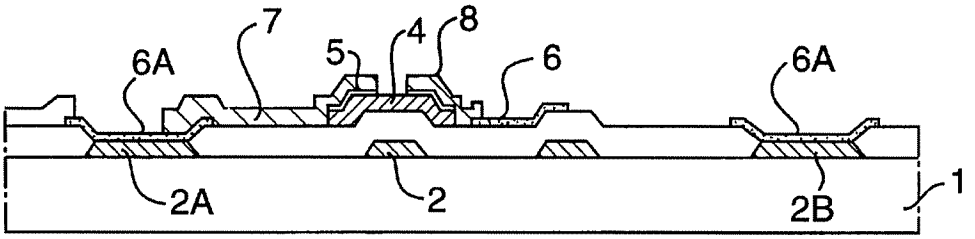


FIG. 1e
PRIOR ART

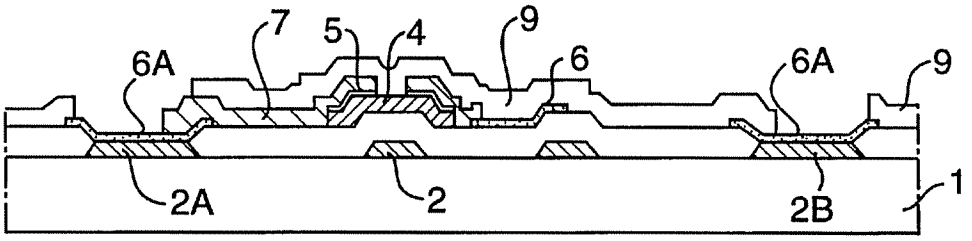


FIG. 1f
PRIOR ART

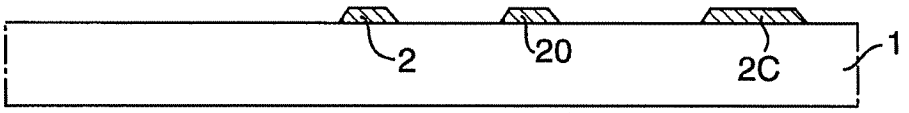


FIG. 2a

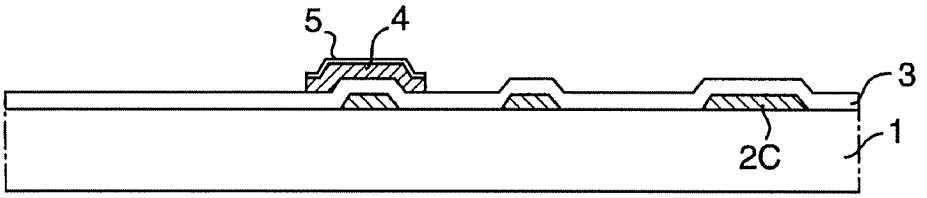


FIG. 2b

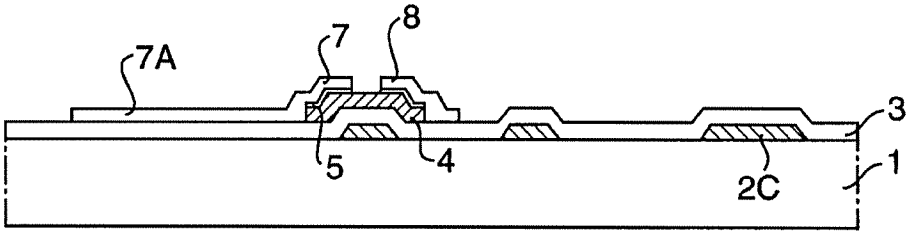


FIG. 2c

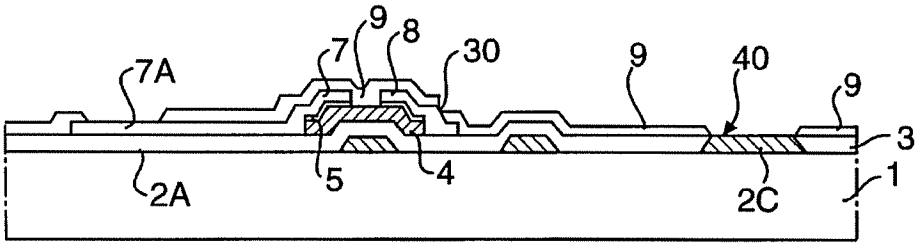


FIG. 2d

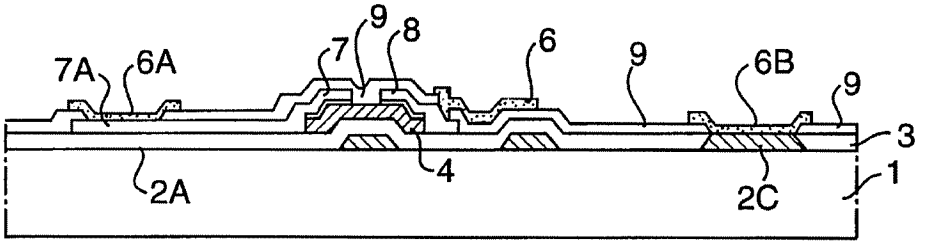


FIG. 2e

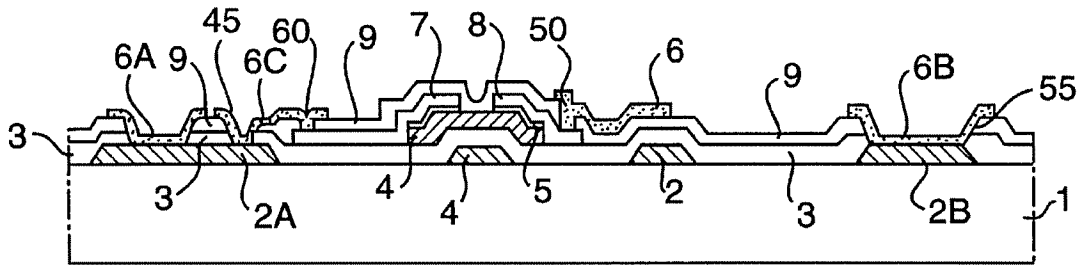


FIG. 3

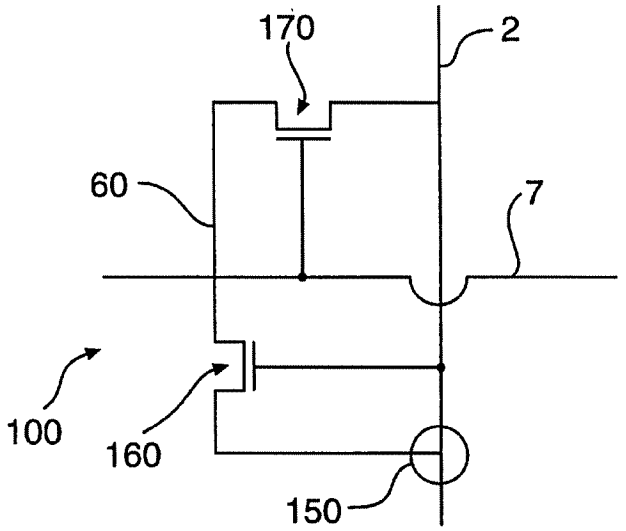


FIG. 4

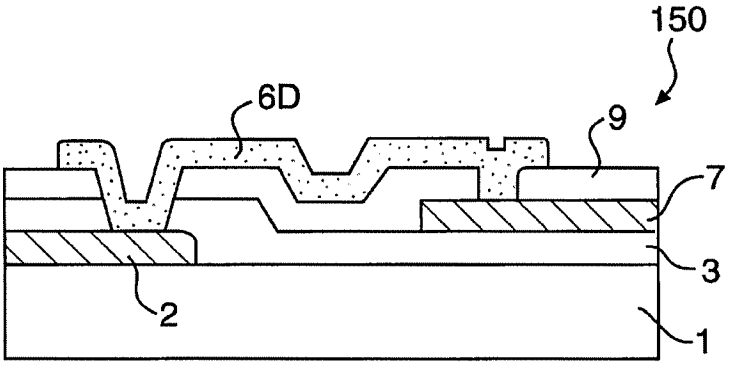


FIG. 5

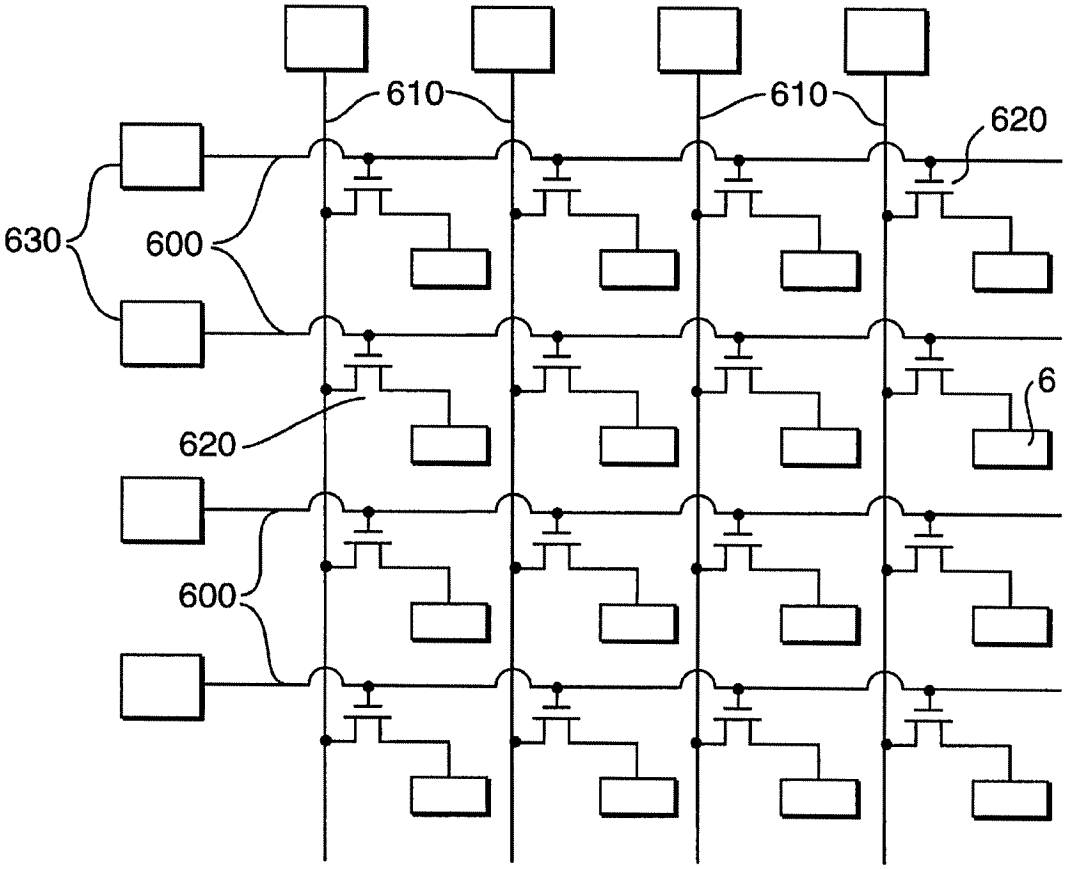


FIG. 6
PRIOR ART

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

This is a continuation of application Ser. No. 08/616,291, Filed Mar. 15, 1996.

BACKGROUND OF THE INVENTION

The present invention relates to a liquid crystal display (LCD) device and a method of manufacturing the same, and more particularly, to a liquid crystal display device having a combined source electrode and source pad structure.

Active matrix thin film displays include thin film transistors (TFTs) for driving the liquid crystal material in individual pixels of the display. As shown in FIG. **6**, a conventional LCD includes an array of pixels each having liquid crystal material (not shown) sandwiched between a common electrode provided on a top plate (not shown) and a pixel electrode **6** disposed on a bottom plate. The bottom plate further includes a plurality of gate lines **600** intersecting a plurality of data lines **610**.

Thin film transistors **620**, serving as active devices, are located at intersecting portions of gate lines **600** and data lines **610**. Gate lines **600** and data lines **610** are connected to the gates and sources, respectively of thin film transistors **620**. In addition, pixel electrodes **6** are connected to respective drain electrodes of thin film transistors **620**. Gate Pads **630** and Data Pads **640** are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively.

A conventional method of manufacturing a liquid crystal display device including TFT driving elements will be described with reference to FIGS. **1***a*–**1***f*.

As shown in FIG. **1***a*, a conductive layer is formed on a transparent glass substrate **1** and patterned to form gate **2**, storage capacitor electrode **2**D, source pad **2**A, and gate pad **2**B. Gate pad **2**B is used for receiving a voltage to drive and active layer in the completed TFT device.

As shown in FIG. **1***b*, a gate insulating film **3**, such as a nitride film or an oxide film, is formed on the entire surface of the substrate in order to electrically insulate gate **2**. An amorphous silicon active layer **4** is formed on a portion of gate insulating film **3** overlying gate **2**. Then, in order to reduce the contact resistance between the active layer and the source/drain regions in the completed device, and appropriately doped semiconductor layer **5** is formed on amorphous silicon layer **4** as an ohmic contact layer. Doped semiconductor layer **5** and amorphous silicon layer **4** are then etched in accordance with a predetermined active layer pattern.

Since a pad wiring layer is necessary in order to communicate information from an external driving circuit to the gate and source, a gate insulating film **3** is selectively etched to expose source pad **2**A and gate pad **2**B (see FIG. **1***c*). Next, as shown in FIG. **1***d*, a transparent conductive layer (ITO) is deposited on the entire surface of the substrate and patterned to form a pixel electrode **6**, which is formed on a portion of the display pixel, while ITO patterns **6**A and **6**B are formed on source pad **2**A and gate pad **2**B, respectively.

As shown in FIG. **1***e*, the TFT is formed on the active layer and includes a conductive layer deposited on the substrate and simultaneously patterned to form source and drain electrodes **7** and **8**, respectively. Source electrode **7** is connected to source pad **2**A, and drain electrode **8** is contact with impurity-doped semiconductor layer **5** and pixel electrode **6**. In the completed device structure, source electrode

7 conducts a data signal, received from a data wiring layer and drain electrode **8**, to pixel electrode **6**. The signal is stored in the form of charge on pixel electrode **6**, thereby driving the liquid crystal.

As shown in FIG. **1***f*, a nitride film is deposited on the entire surface of the substrate as a passivation layer **9** in order to seal the underlying device from moisture and to prevent absorption of impurities. Passivation layer **9** is selectively etched to expose source-pad **2**A and gate pad **2**B, thereby completing the TFT.

In the conventional method described above, The source electrode **7** and pixel electrode **6** provided on the same surface of gate insulating film **3**. Accordingly, processing errors can cause these electrodes to contact each other. As a result, shorts can occur, thereby reducing yields.

Further, since the source pad for the source wiring is composed of the same material as the gate, its contact resistance with the underlying source electrode can be high. In addition, at least six masking steps are required as follows: patterning the gate, storage capacitor electrode, source pad and gate pad; forming the active layer pattern; patterning the gate insulating film for exposing the pad part; forming the pixel electrode; forming the source and drain electrode; and patterning the passivation film for exposing the pad part. Thus, the conventional process requires an excessive number of fabrication steps which increase cost and further reduce yield.

SUMMARY OF THE INVENTION

In order to solve the aforementioned problems, it is an objective of the present invention to provide a liquid crystal display device and a method of manufacturing the same, in which processing errors can be prevented and the Yield can be increased by etching the gate insulating film after the step of forming the passivation layer.

To accomplish this objective of the present invention, there is provided a liquid crystal display device comprising a substrate; a gate electrode; a gate pad and a source pad formed on the substrate as a first conductive layer; a gate insulating film formed on the entire surface of the substrate; a semiconductor layer and an impurity-doped semiconductor layer formed on the gate insulating film above the gate electrode; a source electrode and a drain electrode formed on the semiconductor layer; a passivation layer formed on the entire surface of the substrate; a first contact hole exposing the source pad; a second contact hole exposing a portion of the drain electrode; a third contact hole exposing the gate pad portion; and a fourth contact hole exposing the source electrode, the contact holes being formed by etching the passivation layer and gate insulating film; a pixel electrode connected with the drain electrode through the second contact hole; and a transparent conductive layer connecting the source pad with the source electrode through the first contact hole and fourth contact hole.

To further accomplish the objective of the present invention, there is also provided a method of manufacturing a liquid crystal display device, comprising the steps of forming a first conductive layer on a substrate; patterning the first conductive layer to respectively form a gate electrode, a gate pad and a source pad; sequentially forming an insulating film, a semiconductor layer and an impurity-doped semiconductor layer on the entire surface of the substrate; patterning the impurity-doped semiconductor layer and semiconductor layer to an active pattern; forming a second conductive layer on the entire surface of the substrate; patterning the second conductive layer to form a

source electrode and a drain electrode; forming a passivation film on the entire surface of the substrate; Selectively etching the passivation film and insulting film to respectively form a first contact hole exposing the source pad, a second contact hole exposing a portion of the drain electrode, a third contact hole exposing a gate pad portion, and a fourth contact hole exposing a portion of the source electrode; forming a transparent conductive layer on the entire surface of the substrate; and patterning a pixel electrode connected with the drain electrode through the second contact hole, a transparent conductive layer connected with the gate pad through the third contact hole, and a transparent conductive layer connecting the source pad with the source electrode through the first and fourth contact holes.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

FIG. **1***a* to if are cross-sectional views illustrating steps of a conventional method for manufacturing a liquid crystal display device;

FIGS. **2***a* to **2***e* are cross-sectional views illustrating steps of a method for manufacturing a liquid crystal display according to a preferred embodiment of the present invention;

FIG. **3** is a cross-sectional view illustrating a liquid crystal display device structure according to a second embodiment of the present invention;

FIG. **4** is a circuit diagram of one example of a liquid crystal display device in which a gate material is connected with a source material in accordance with a third embodiment of the present invention; and

FIG. **5** is a vertical-cross-sectional view of the device shown in FIG. **4**.

FIG. **6** is a plan view schemetic representation of one prior embodiment of a matrix display.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, preferred embodiments of the present invention will be described with reference to the attached drawings.

Referring first to FIG. **2***a*, a conductive layer is formed on a transparent glass substrate **1** and patterned to form a gate electrode **2**, a storage capacitor electrode **2**D, and a gate pad **2**C, all of the same material. The gate electrode is used for applying a voltage in order to drive the active layer in the completed TFT device.

As shown in FIG. **2***b*, a gate insulating film **3** such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate **2**. Semiconductor active layer **4** is then formed on insulating gate **2**. Active layer **4** is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resistance between the active layer and the subsequently formed source and drain, an impurity-doped semiconductor layer **5** is formed on amorphous silicon layer **4**, as an ohmic contact layer. Impurity-doped semiconductor layer **5** and amorphous silicon layer **4** are etched according to a predetermined active layer pattern.

As shown in FIG. **2***c*, a conductive layer for forming source electrode **7** and drain electrode **8** is deposited on the substrate by patterning a sputtered layer of conductive material. Using the source and drain electrodes as masks, portions of the impurity-doped semiconductor layer **5** are exposed and then etched. Source electrode **7** thus forms part of a transistor region and serves as source pad **7**A above the gate insulating film so that the same conductive layer constitutes part of the source wiring and the source electrode of the TFT.

As shown in FIG. **2***d*, a passivation layer **9**, e.g., a nitride film, is deposited on the entire surface of the substrate by a CVD process. Then, a predetermined portion of passivation layer **9** and gate insulating film **3** are selectively etched to form first, second and third contact holes **20**, **30** and **40**, thereby exposing a predetermined region of source pad **7**A above gate insulating film **3**, a predetermined region of drain electrode **8**, and a predetermined region of gate pad **2**C. For external electrical connections It is necessary to exposed pads **7**A and **2**C.

As shown in FIG. **2***e*, an indium tin oxide (ITO) layer is next deposited on the substrate by sputtering or a CVD process and etched according to a predetermined pattern to form a pixel electrode **6**. As further shown in FIG. **2***e*, pixel electrode **6** is connected to the upper portion of drain electrode **8** At the same time, ITO pattern **6**B is formed on gate pad **2**C. In addition, ITO pattern **6**A is provided on source pad **2**A, which is part of a data electrode of the LCD. The TFT of the present invention having electrical contacts or wiring structures including gate pad **2**C, layer **6**B and layer **6**A, source pad **7**A is thus completed.

As described above, the pixel electrode **6** is formed after the passivation process in the present invention. In contrast, pixel electrode **6** is formed after the pad process or the source/drain formation process in the conventional method. Thus, the passivation layer is interposed between the source/drain formation material and the pixel electrode, thereby effectively isolating these layers and preventing shorts.

Further, unlike the conventional process, the method in accordance with the present invention does not require the step of exposing the pad directly after depositing the gate insulating film, and the source and gate pads are exposed by etching during the passivation process. Thus, the pixel electrode, which is made of ITO, is formed on the source and gate pads. In addition, the source pad is not formed of gate material, but is formed from the source formation material, while the source and drain are deposited. Thus, the problem of high contact resistance between the source pad and the source, caused by forming the source pad from the gate material, can be avoided.

FIG. **3** illustrates a second embodiment of the present invention in which the step of etching the gate insulating layer and the step of etching the passivation layer to expose the pads are preformed in only one mask step. In particular, source pad **2**A is composed of gate material, as in the conventional method, and is formed at the same time as gate **2**, storage capacitor electrode **2**D and gate pad **2**B. After forming first, second, third and fourth contact holes **45**, **50**, **55** and **60**, material for forming the pixel electrode is then deposited. As a result, since both the first (**45**) and fourth (**60**) contact holes are formed over source pad **2**A (formed of the same material as the gate) and source electrode **7**, respectively, the source electrode **7** and source pad **2**A may be connected to each other in the same step that the pixel electrode is formed. Thus, after patterning, a first transparent conductive layer **6**C connects source electrode **7** with source pad **2**A, and a second transparent conductive layer **6** (i.e., the pixel electrode) is connected to drain electrode **8**.

In other words, a conductive layer is formed on a transparent glass substrate **1** and patterned to form gate **2**, a storage capacitor electrode **2**D,. a source pad **2**A and a gate

pad 2B. After forming a gate insulating film 3 on the entire surface of the substrate, an amorphous silicon layer 4 and an impurity-doped semiconductor layer 5 are sequentially formed therson. These layers are then etched in accordance with a predetermined active layer pattern.

Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8. After forming a passivation layer 9 on the entire surface of the substrate, passivation layer 9 and gate insulating film 3 are selectively etched, thereby forming a first contact hole exposing the source pad 2A and a third contact hole exposing the gate pad 2B. Since the passivation layer 9 and gate insulating film 3 are preferably etched in a single step, the sidewalls of the first and second contact holes are planar and smooth.

ITO is then deposited on the entire surface of the substrate and patterned to form a pixel electrode 6 connected to drain electrode 8 through the contact hole overlying drain electrode 8 in the pixel part. At the same time, ITO patterns 6A, 6B and 6C are formed to contact source pad 2A and gate pad 2B through the contact holes formed at gate insulating film 3 and passivation layer 9.

Further, in accordance with an additional embodiment of the present invention, a repair line or static electricity protection circuit can also be provided during deposition of the pixel electrode layer. FIG.4 is a schematic diagram of static electricity protection circuit 100, and FIG.5 is an enlarged cross-sectional view of a portion 150,of the circuit.

In the circuit shown in FIG.4. if a high potential due to an electrostatic discharge is present on source electrode 7, for example, transistor 170 is rendered conductive to discharge source electrode 7 to gate line 2. Similarly, gate line 2 can discharge to source electrode 7 via transistor 160. As shown in FIG.5, the connection between gate line 2 and source electrode 7 is achieved by forming contact holes in insulative films 3 and 9 and then depositing conductive material (preferabel ITO) into these holes while forming the pixel electrode.

According to the present invention as described above, the manufacture of the TFT of the liquid crystal display device can be accomplished using five mask steps (step of forming the gate, step of forming the active layer, step of forming the source and drain, step of etching the passivation layer and gate insulating film, and step of forming the pixel electrode), while the conventional process requires six or more mask steps. Thus, manufacturing cost can be reduced.

Further, when the source pad is formed from the same material as the source electrode, the contact resistance problem caused when the source pad is in contact with the source electrode can be solved. In addition, since the pixel electrode is formed after forming the passivation layer, processing errors resulting in the pixel electrode contacting the source and drain can be prevented.

Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

What is claimed is:

1. A wiring structure comprising:

a substrate;

a first conductive layer formed on a first portion of said substrate;

a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

a second conductive layer formed on a first portion of said first insulative layer;

a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;

an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

2. A wiring structure comprising:

a substrate;

a first conductive layer formed on a portion of said substrate;

a first insulative layer having a first via hole exposing a portion of said first conductive layer;

a second conductive layer formed on a portion of said first insulative layer;

a second insulative layer having a second via hole exposing said exposed portion of the first conductive layer and having a third via hole exposing a portion of the second conductive layer;

a third conductive layer formed on said second insulative layer and electrically connecting said first conductive layer to said second conductive layer through said first, second, and third via holes,

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

3. A wiring structure in accordance with claim 2, wherein said third conductive layer includes indium tin oxide.

4. A wiring structure in accordance with claim 2, wherein said first and second via holes constitute a common hole exposing said exposed portion of said first conductive layer, a sidewall of said common hole being substantially smooth.

5. A wiring structure in accordance with claim 2, wherein said second via hole is aligned with said first via hole.

6. A liquid crystal display device comprising:

a substrate having a primary surface;

a first conductive layer disposed on a predetermined region of said primary surface;

a first insulating layer formed overlying said primary surface including said first conductive layer, said first insulating layer including a first contact hole exposing a predetermined portion of said first conductive layer;

a second conductive layer formed on a predetermined region of said first insulating layer;

a second insulating layer formed overlying said primary surface including said second conductive layer, said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region; and

a third conductive layer formed on said second insulating layer and electrically connected to said first and second conductive layers via said first and second contact holes,

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

7. A liquid crystal display device in accordance with claim **6**, wherein said third conductive layer includes material suitable for forming a pixel electrode.

8. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer pattern on a substrate, said first conductive layer pattern being connected to a first terminal of a thin film transistor;

forming a first insulating layer overlying a surface of said substrate including said first conductive layer pattern;

forming a second conductive layer pattern on said first insulating layer, said second conductive layer pattern being connected to a second terminal of the thin film transistor;

forming a second insulating layer overlying said substrate including said second conductive layer pattern;

selectively etching said first and second insulating layers to form a first contact hole and a second contact hole exposing said first conductive layer pattern and said second conductive layer pattern, respectively; and

forming a third conductive layer on said second insulating layer, said third conductive layer electrically connected to said first and second conductive layer patterns via said first and second contact holes, respectively.

9. A method of manufacturing a liquid crystal display device in accordance with claim **8**, wherein said selective etching step is performed in a single etch step and said third conductive layer includes indium tin oxide.

10. A liquid crystal display device comprising:

a substrate;

a first conductive layer on said substrate including:
a gate electrode,
a gate pad, and
a source pad;

a gate insulating film on said surface of said substrate,

a portion of said gate insulating film overlying said gate electrode;

a semiconductor layer on said portion of said gate insulating film;

an impurity-doped semiconductor layer on said semiconductor layer;

a source electrode and a drain electrode on said semiconductor layer;

a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;

a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

a second contact hole provided through said passivation layer exposing said drain electrode;

a third contact hole provided through said passivation layer and said gate insulating film exposing said gate pad;

a fourth contact hole provided through said passivation layer exposing said source electrode;

a pixel electrode electrically connected with said drain electrode via said second contact hole; and

a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

11. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer on a substrate;

patterning said first conductive layer to form a gate electrode, a gate pad and a source pad;

forming an insulating film on said substrate including said patterned conductive layer;

forming a semiconductor layer on said insulating film;

forming an impurity-doped semiconductor layer on said semiconductor layer;

patterning said impurity-doped semiconductor layer and said semiconductor layer to form an active layer;

forming a second conductive layer overlying said substrate including said active layer;

patterning said second conductive layer to form source electrode and a drain electrode on said active layer;

forming a passivation film overlying said substrate including said source pad, a portion of said drain electrode, said gate pad portion, and a portion of said source electrode;

selectively etching said passivation film and said insulating film to form a first contact hole exposing said source pad, a second contact hole exposing said portion of said drain electrode, a third contact hole exposing said gate pad portion, and a fourth contact hole exposing said portion of said source electrode;

patterning a pixel electrode electrically connected to said drain electrode via said second contact hole;

patterning a first transparent conductive layer electrically connected to said gate pad through said third contact hole; and

patterning second transparent conductive layer electrically connecting said source pad to said source electrode via said first and fourth contact holes.

* * * * *

EXHIBIT C

United States Patent [19]

Shimbo

[11] **Patent Number: 4,624,737**

[45] **Date of Patent: Nov. 25, 1986**

[54] **PROCESS FOR PRODUCING THIN-FILM TRANSISTOR**

[75] Inventor: **Masafumi Shimbo, Tokyo, Japan**

[73] Assignee: **Seiko Instruments & Electronics Ltd., Tokyo, Japan**

[21] Appl. No.: **743,092**

[22] Filed: **Jun. 10, 1985**

[30] **Foreign Application Priority Data**

Aug. 21, 1984 [JP] Japan 59-173848

[51] **Int. Cl.**[4] **H01L 21/306; B44C 1/22; C03C 15/00; C23F 1/02**

[52] **U.S. Cl.** ..... **156/643;** 29/576 R; 29/578; 29/591; 156/652; 156/653; 156/656; 156/657; 156/659.1; 156/662; 156/667; 357/4; 357/23.1; 427/88; 427/93; 427/94

[58] **Field of Search** ..... 156/643, 646, 652, 653, 156/655, 656, 657, 659.1, 661.1, 662, 667, 668; 204/192 E, 192 EC; 427/38, 39, 88, 89, 90, 93, 94, 95; 430/313, 317, 318; 29/571, 576 R, 578, 591; 357/4, 23.1, 23.7, 65, 71

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Primary Examiner—William A. Powell
Attorney, Agent, or Firm—Robert E. Burns; Emmanuel J. Lobato; Bruce L. Adams

[57] **ABSTRACT**

A gate insulating film, a high-resistivity semiconductor film, a low-resistivity semiconductor film and if necessary a conducting film are successively deposited in lamination without exposing them to any oxidizing atmosphere including atmospheric air, and then the source and drain electrodes are selectively formed.

4 Claims, 13 Drawing Figures

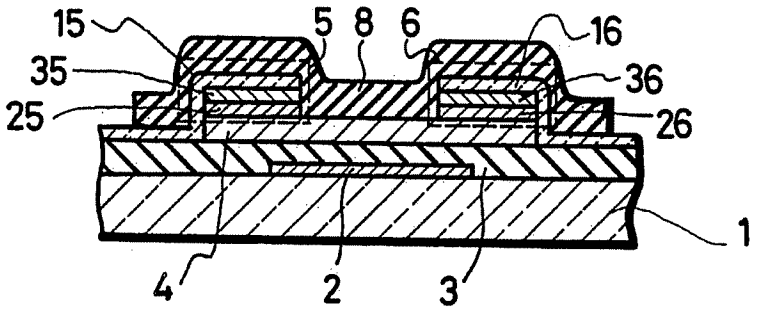


FIG. 1a PRIOR ART

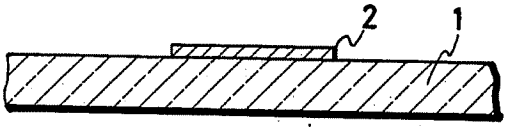


FIG. 1b PRIOR ART

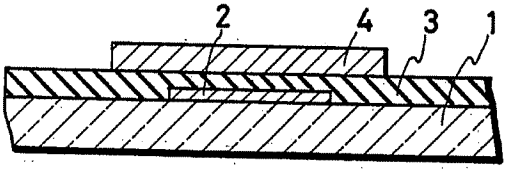


FIG. 1c PRIOR ART

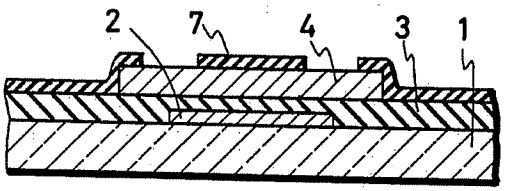


FIG. 1d PRIOR ART

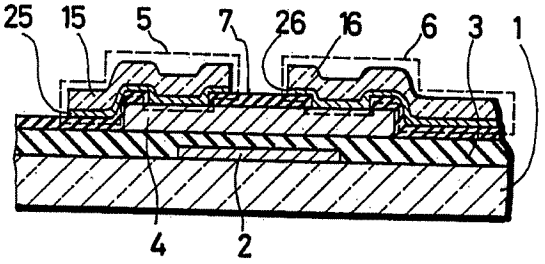


FIG. 2a

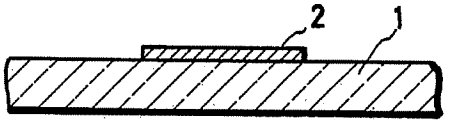


FIG. 2b

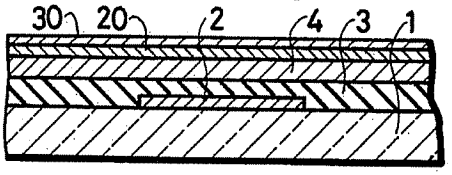


FIG. 2c

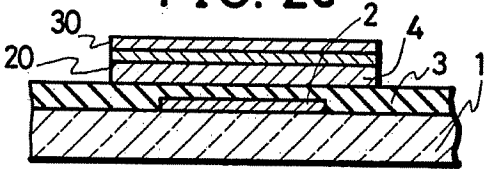


FIG. 2d

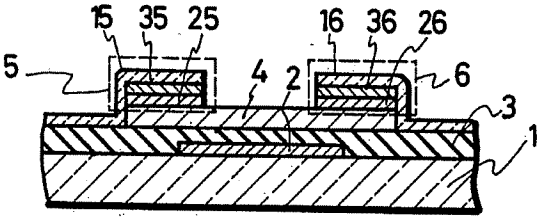


FIG. 2e

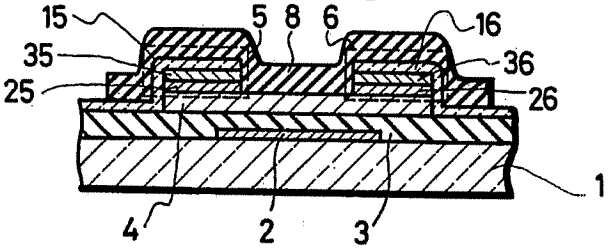


FIG. 3a

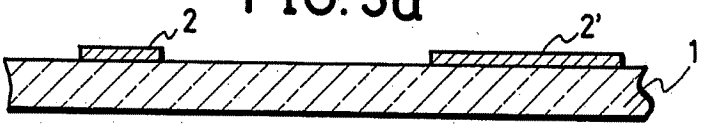


FIG. 3b

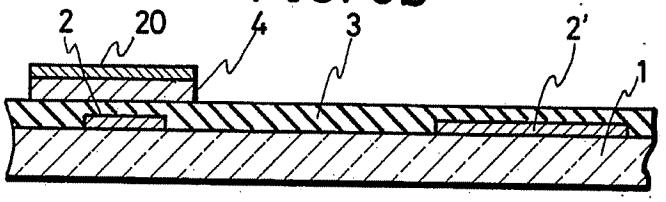


FIG. 3c

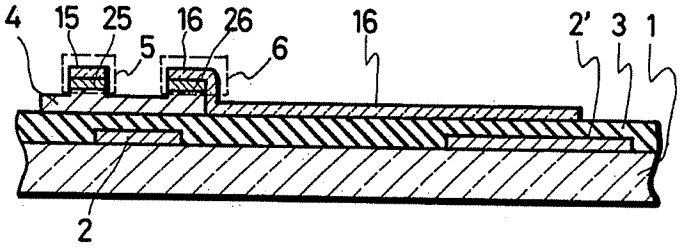
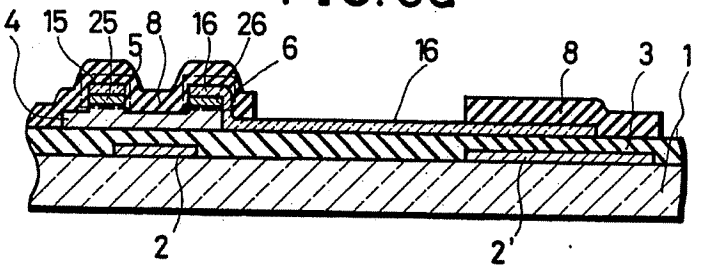


FIG. 3d



PROCESS FOR PRODUCING THIN-FILM TRANSISTOR

BACKGROUND OF THE INVENTION

This invention relates to a process for producing a thin-film transistor with improved performance.

Thin-film transistors (TFT) using semiconductor films of amorphous silicon (a-Si) or polycrystalline silicon (P-Si) are being applied to liquid crystal displays and like devices. Such thin-film transistors are diversified in structure. FIGS. **1***a* to **1***d* illustrate a conventional process for producing a thin-film transistor of a planar structure using amorphous silicon film. Shown in FIG. **1***a* in a sectional view is the initial step for selectively forming a gate electrode **2** on an insulating substrate **1** such as a glass substrate. Then, as shown in FIG. **1***b*, a gate insulating film **3** (such as silicon nitride film) and an amorphous silicon film **4** are continuously deposited, and said amorphous silicon film **4** is selectively etched. Then a field insulating film **7** (such as SiOx film) is deposited and windows for contact with source and drain regions are formed as shown in FIG. **1***c*. Although not shown, a gate contact window is also formed simultaneously. Thereafter, as illustrated in FIG. **1***d*, for instance n^+ amorphous silicon films **25**, **26** and metal (such as Al) films **15**, **16** are deposited and selectively etched to form drain and source electrodes **5**, **6**, thereby completing a thin-film transistor unit. If necessary, a surface passivation film and/or light-shielding film are further formed thereon.

In the conventional process shown in FIGS. **1***a* to **1***d*, since the masking step precedes the deposition of n^+ amorphous films **25**, **26**, natural oxide is produced on the exposed surface of amorphous silicon film **4**. Although such natural oxide can be removed by an aqueous solution of hydrofluoric acid (HF) or a similar substance, the possibility is still great that oxygen and its compounds as well as other impurities can collect on the laminate surface as it is exposed to the atmosphere. This would give rise to electrical resistance between the source and drain and between channels in the thin-film transistor thus obtained, making such transistor unable to exhibit its desired characteristics. A similar phenomenon would also occur at the interface of n^+ amorphous silicon films **25**, **26** and metal films **15**, **16**.

As described above, according to the conventional process, resistance would be generated between the source and drain and between channels and it was thus impossible to obtain the proper current flow and frequency characteristics. It was also a disadvantage of such conventional process that it was necessary to repeat the masking step as many as 5 to 6 times.

SUMMARY OF THE INVENTION

It is an object of present invention to provide a simplified process for producing a thin-film transistor with an improved contact arrangement.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1***a* to **1***d* are sectional views showing the sequential steps in a conventional thin-film transistor production process.

FIGS. **2***a* to **2***e* are sectional views illustrating stepwise a process for producing a thin-film transistor according to the present invention.

FIGS. **3***a* to **3***d* are sectional views illustrating the sequential steps for producing a thin-film transistor according to the process of this invention as it was applied to a substrate for liquid crystal display.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will be described in detail below with reference to the accompanying drawings.

FIGS. **2***a* to **2***e* are sectional views illustrating a process for producing a thin-film transistor using amorphous silicon according to this invention. FIG. **2***a* shows in a sectional view the initial step for selectively forming a gate electrode **2** on an insulating substrate **1** such as glass, quartz, ceramic, insulator-coated silicon or metal. Metals such as Cr, Mo, W, Al, Ta, etc., and their silicides, impurity-doped polysilicon and other like materials can be used as said gate electrode **2**.

In the next step illustrated in FIG. **2***b* in a sectional view, a gate insulating film **3**, a high-resistivity film **4**, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film **20** and a conducting film **30** made of a metal or other material are successively formed on said gate electrode **2** and substrate **1** without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by forming a silicon nitride (SiNx) film as gate insulating film **3** from a mixed gas of SiH_4 and NH_3, forming a high-resistivity a-Si:H film **4** by using SiH_4 and forming a n^+ a-Si:H film **20** from a mixed gas of PH_3 and SiH_4 in the same evacuated chamber in a plasma CVD apparatus. It is also possible to form said films successively in the respective chambers by using a plasma CVD apparatus having in-line chambers. Further, when a sputtering or metalizing chamber is additionally provided, conducting film **30** can be also deposited continuously without exposure to the atmosphere. Beside SiNx, a film of SiOx or a multi-layer film made of such materials can be used as said gate insulating film **3**. In place of said high-resistivity amorphous silicon film **4**, there can be used a film of amorphous silicon-fluorine alloy (a-Si:F) or amorphous silicon-hydrogen-fluorine alloy (a-Si:H:F) using, for instance, SiF_4, or a microcrystalline amorphous silicon film. Such alloys can be also used for said low-resistivity amorphous silicon film **20**, and such film may contain other impurites beside phosphorous impurities. As said conducting film **30**, it is desirable to use a stable conducting film such as a transparent conducting film made of a refractory metal such as Cr, W, Mo, Ta, etc., and silicides thereof, or indium-tin-oxide (ITO), SnO_2 and the like. Use of a transparent conducting film has the advantage that the process is simplified when the thin-film transistor of this invention is applied to an active matrix liquid crystal display.

FIG. **2***c* illustrates the step in which said conducting film **30**, low-resistivity amorphous silicon film **20** and high-resistivity amorphous silicon film **4** are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step. Then, as illustrated in FIG. **2***d* in a sectional view, drain and source electrode members **15**, **16** are selectively provided, and conducting film **30** and low-resistivity amorphous silicon film **20** shown in FIG. **2***c* are selectively removed with said electrode members **15**, **16** serving at least as a part of the mask to form drain electrode **5** and source electrode **6**. In this step, it is desirable to clean the surface of conducting film **30** by proper etching means such as sputter etching or ion

etching before forming said drain and source electrode members **15, 16**. In this case, the channel areas of the thin-film transistor are safe from damage by cleaning as they are covered with conducting film **30**. The same materials as used for conducting film **30** and other materials such as Al can be used for said drain and source electrode members **15, 16**. When selectively etching low-resistivity amorphous silicon film **20**, no problem arises even if it is overetched to the extent that etching reaches the high-resistivity amorphous silicon film **4**.

In the final step illustrated in FIG. 2*e*, a surface passivation film **8** is deposited, and the drain and source electrodes **15, 16** and gate electrode **2** are partly exposed (not shown). A CVD film of SiOx, SiNx, etc., a resist or a coating of polyimide resin can be used as said surface passivation film **8**. If light shielding is required, a multilayer film composed of said insulating film and a metal or high-resistivity semiconductor film can be used as said surface passivation film **8**. When amorphous silicon-germanium alloy ($a\text{-}Si_{1-x}Ge_x$) is used as light-shielding film, surface passivation may not be necessary.

FIGS. 3*a* to 3*d* show sectionally a unit picture cell in an application of the present invention to the manufacture of a TFT substrate for liquid crystal display. FIG. 3*a* illustrates a step in which gate electrode **2** extending along one line and gate electrodes **2'** on another line are formed on a transparent insulating substrate **1** such as glass substrate. Then, as illustrated in FIG. 3*b*, gate insulating film **3**, high-resistivity amorphous silicon film **4** and low-resistivity amorphous silicon film **20** are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film **20** and high-resistivity amorphous silicon film **4** are left as an island region in the area where a thin-film transistor is to be formed.

In the next step illustrated in FIG. 3*c*, a transparent conducting film such as ITO film is deposited; then, drain electrode **15** and source electrode **16** which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film **20** is removed. In this example, a charge-holding capacitor is formed by said picture cell electrode (source electrode) **16**, gate electrode **2'** and gate insulating film **3**. In the final step shown sectionally in FIG. 3*d*, surface passivation film **8** concurrently serving as a light-shielding film is deposited and then selectively etched to expose picture cell electrode, drain electrode **15** and a part of gate electrodes **2, 2'** (not shown). In this example, no conducting film is formed on low-resistivity amorphous silicon film **20**, but a conducting film such as ITO film may be formed on said low-resistivity film **20** as in the example shown in FIG. **2**.

As described above, according to the present invention, no oxides, etc., are formed at the interface of high-resistivity amorphous silicon film **4** and low-resistivity amorphous silicon film **20**, so that a good junction can be formed. The same is true with the interface of low-resistivity amorphous silicon film **20** and conducting film **30**. Further, since the interfaces of low-resistivity amorphous silicon film **20** or conducting film **30** and drain and source electrodes **15, 16** can be cleaned without damaging the high-resistivity amorphous silicon film, a good contact can be obtained without sacrificing the inherent properties of thin-film transistor.

According to the present invention, as explained above, a thin-film transistor having good contact characteristics can be formed with only four masking operations. The present invention is especially effective for the production of thin-film transistors requiring a low temperature process such as thin-film transistors using amorphous silicon. It is thus possible with the present invention to obtain a thin-film transistor with small channel series resistance which improves driving performance and frequency characteristics.

While the present invention has been principally described regarding an embodiment thereof as applied to the production of a thin-film transistor using amorphous silicon by utilizing plasma CVD, the invention can as well be applied to the manufacture of thin-film transistors using semiconductor films by utilizing the photo CVD or molecular beam and/or the ion beam deposition method, thin-film transistors using polysilicon, and thin-film transistors using semiconductor films of other materials than silicon; consequently, the present invention is of great industrial significance.

I claim:

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said high-resistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

2. A process for producing a thin-film transistor according to claim **1**, wherein in said second step said conducting film is composed of at least two layers consisting of a low-resistivity semiconductor film and thereon a refractory metal film or transparent conducting film, and both of said films are continuously deposited without being exposed to the oxidizing atmosphere.

3. A process for producing a thin-film transistor according to claim **1** , wherein in said sixth step a light-shielding film is formed at a part of said surface passivation film.

4. A process for producing a thin-film transistor according to claim **2** , wherein in said sixth step a light-shielding film is formed at a part of said surface passivation film.

* * * * *

EXHIBIT D

US006976781B2

(12) **United States Patent**
Chu et al.

(10) **Patent No.: US 6,976,781 B2**
(45) **Date of Patent: Dec. 20, 2005**

(54) **FRAME AND BEZEL STRUCTURE FOR BACKLIGHT UNIT**

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(73) Assignee: **AU Optronics Corp.**, Hsinchu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 31 days.

(21) Appl. No.: **10/446,103**

(22) Filed: **May 28, 2003**

(65) **Prior Publication Data**

US 2004/0080952 A1 Apr. 29, 2004

(30) **Foreign Application Priority Data**

Oct. 25, 2002 (TW) ..... 91125324 A

(51) **Int. Cl.**[7] **F21V 7/04**

(52) **U.S. Cl.** **362/633**; 349/58; 40/209; 40/781

(58) **Field of Search** 362/23, 26, 28, 362/31, 551, 559, 560, 561, 362, 367, 368, 362/374, 382, 396, 433, 444, 600, 632, 633, 362/634; 349/58, 60, 56; 385/129; 40/204, 40/209, 124.02, 661.02, 541, 549, 700, 714, 40/781

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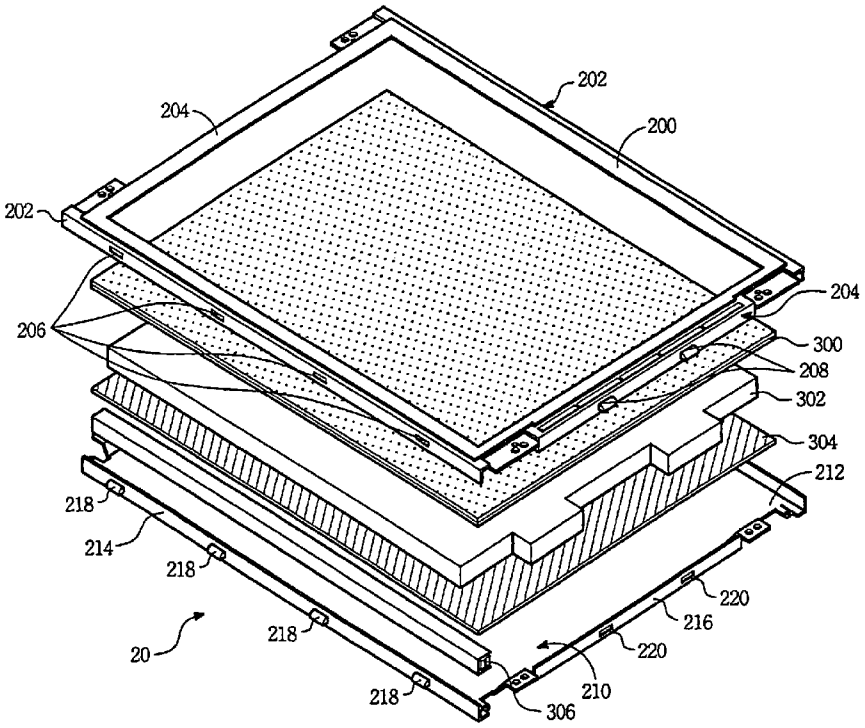
Primary Examiner—Thomas M. Sember
Assistant Examiner—Ismael Negron
(74) *Attorney, Agent, or Firm*—Troxell Law Office, PLLC

(57) **ABSTRACT**

A frame including a first edge and a second edge, wherein on outer surfaces of the first edge, first hooks are formed to protrude outwardly, and on outer surfaces of the second edge, first holes are formed. A bezel has a first sidewall and a second sidewall, wherein on the first sidewall, second holes are formed, and on outer surfaces of the second sidewall, second hooks are formed to protrude outwardly. When the frame is mounted onto the bezel, the first edge is disposed onto inside surfaces of the first sidewall, and the first hooks are inserted and engaged in the second holes for fastening the frame and bezel, simultaneously the second edge is disposed onto the outside surfaces of the second sidewall, and the second hooks are inserted and engaged in the first holes for fastening the frame and the bezel.

13 Claims, 5 Drawing Sheets



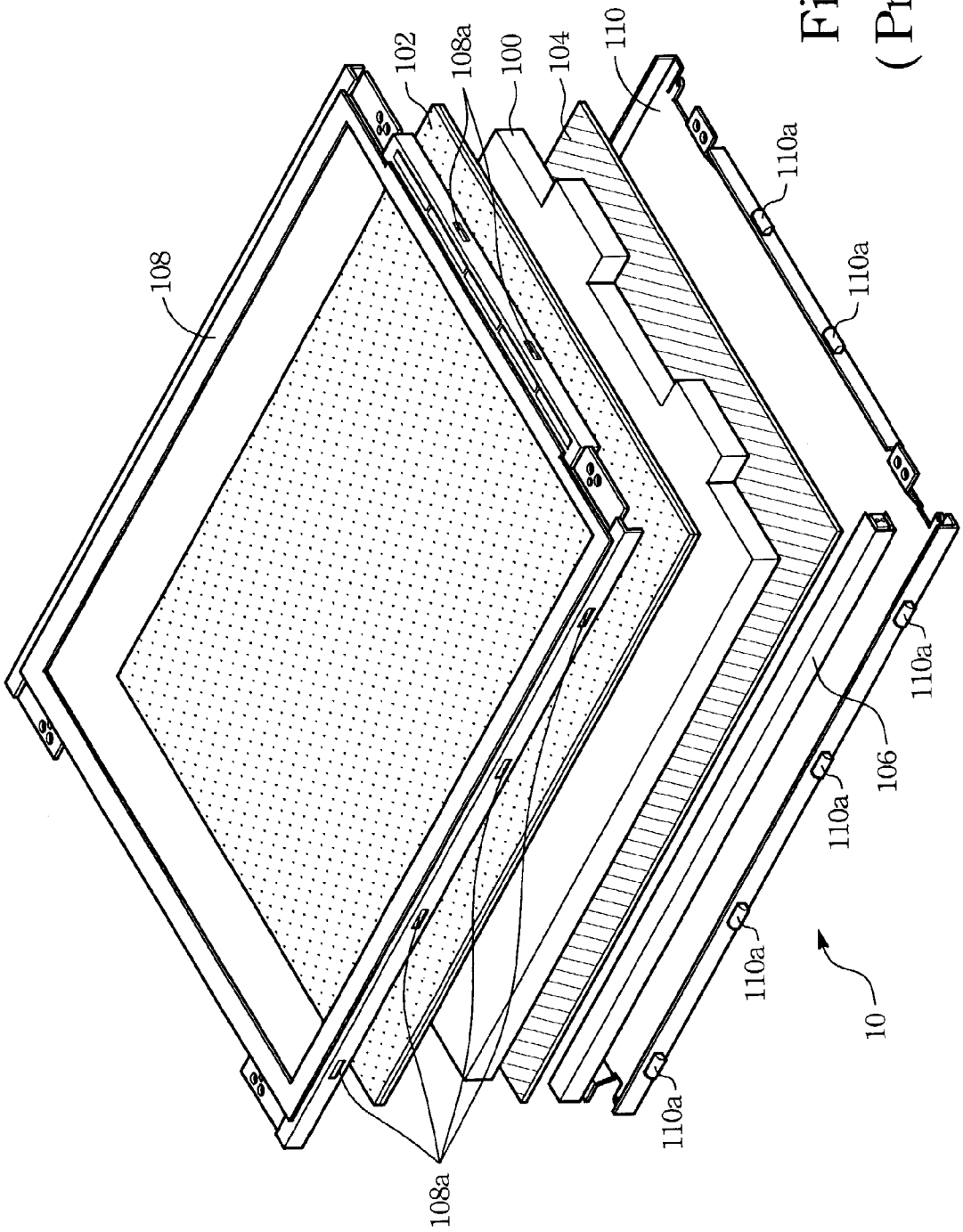


Figure 1
(Prior Art)

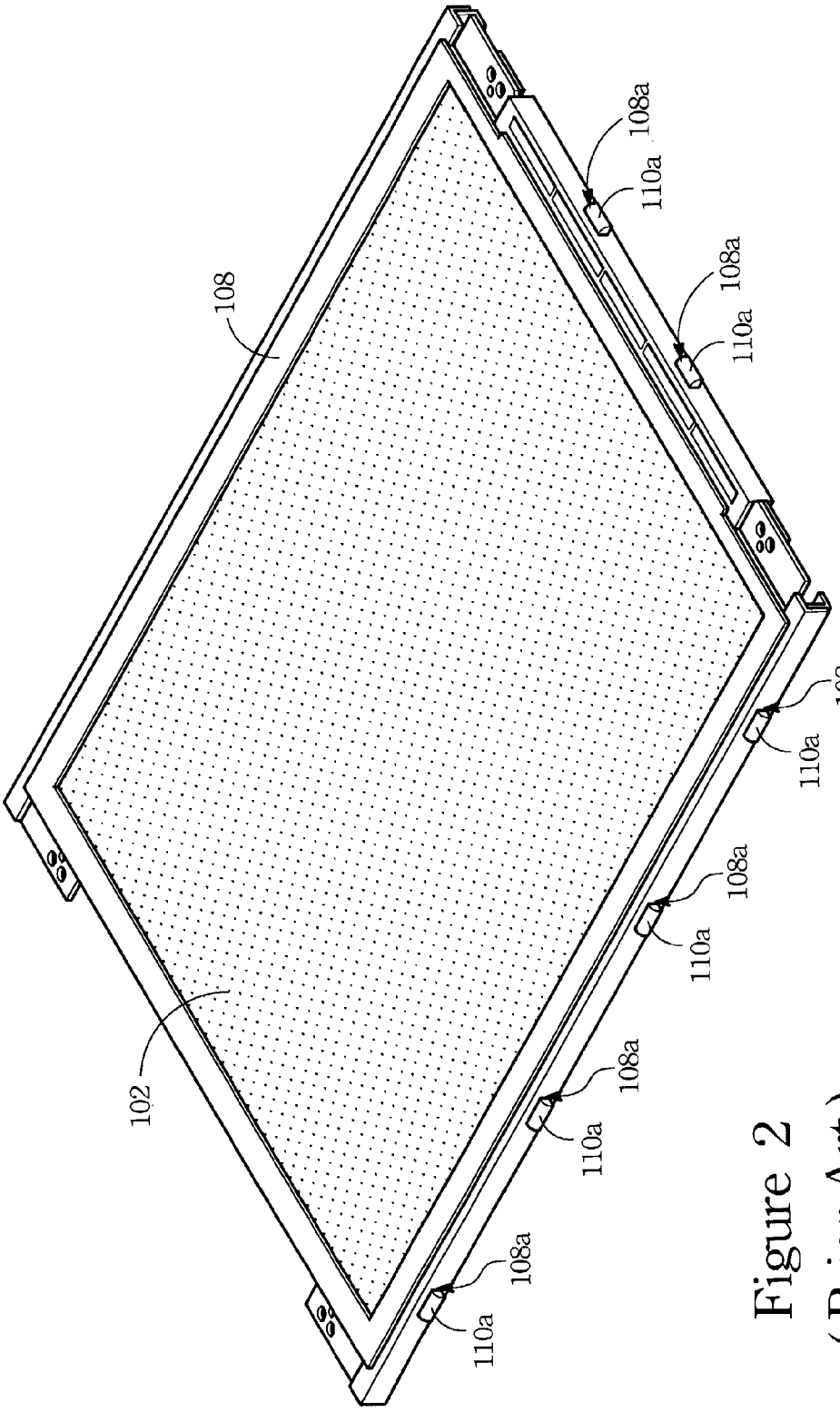


Figure 2
(Prior Art)

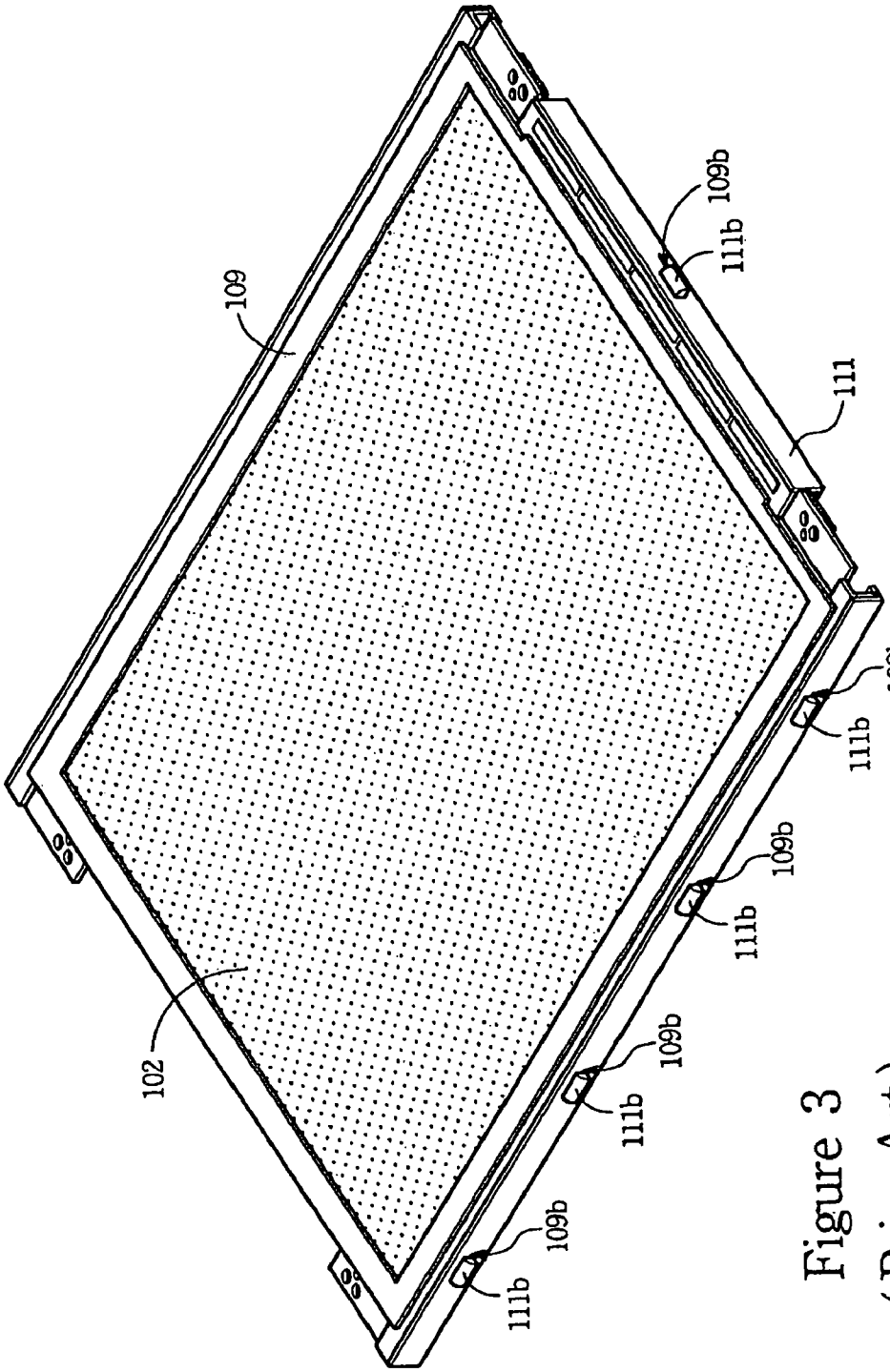


Figure 3
(Prior Art)

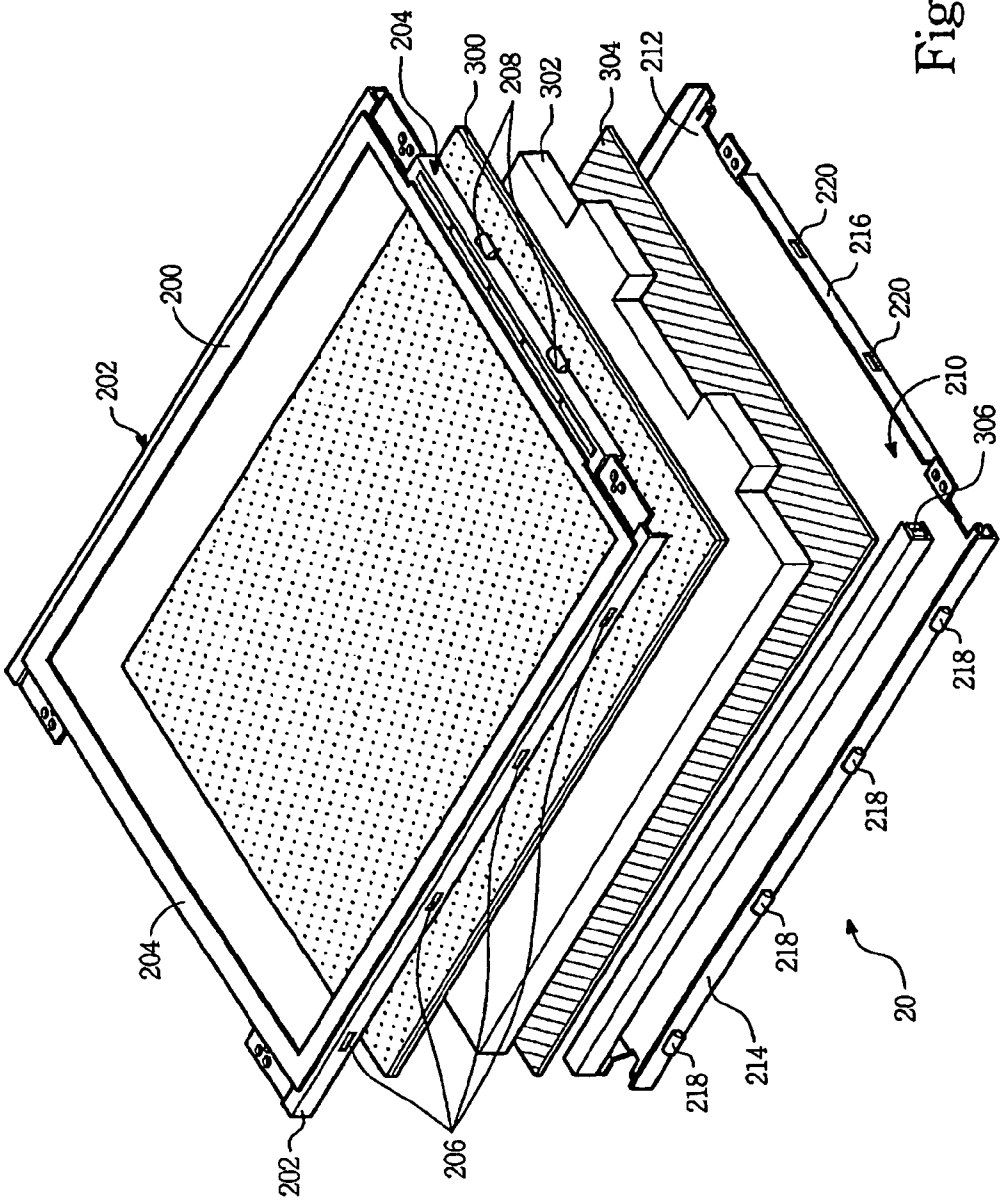

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Figure 4

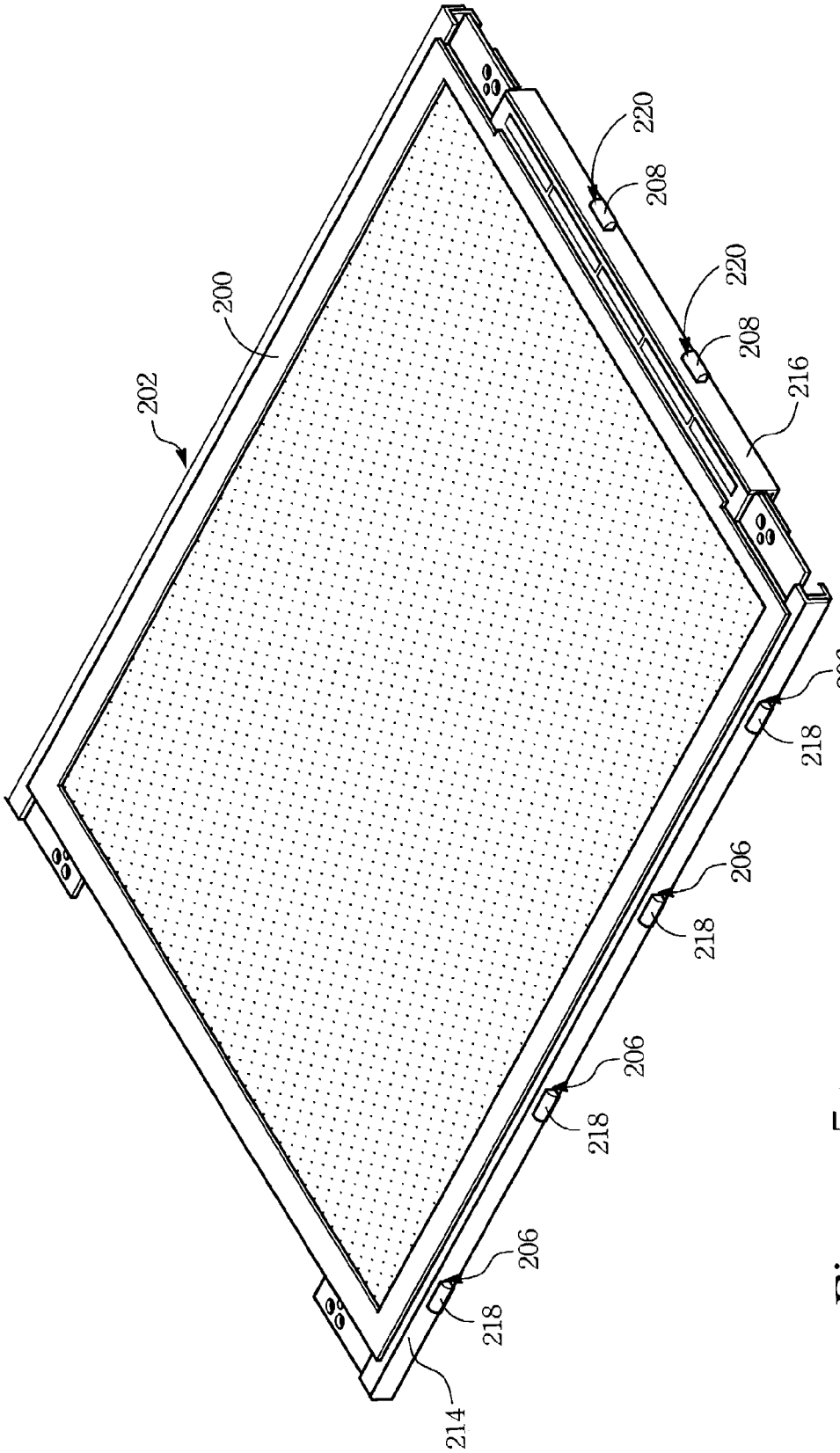

Figure 5

FRAME AND BEZEL STRUCTURE FOR BACKLIGHT UNIT

FIELD OF THE INVENTION

The present invention relates to a backlight unit of a liquid crystal display, and more specifically, to a new assembling manner for mounting a frame onto a bezel to provide the assembling structure the reinforced supporting strength and to provide the convenience of disassembling the frame from the bezel.

BACKGROUND OF THE INVENTION

With the advance of techniques for manufacturing thin-film transistors, the liquid crystal displays (LCD) are widely applied in electrical products, such as PDAs, laptops, digital cameras, cell phones, high resolution television sets, etc. due to advantages as portability, non-radiation and saving electricity. Especially when the manufactures devote themselves to further research and improve the materials, processes and equipments for producing LCD devices, the qualities of the LCDs are promoted and prime costs are reduced substantially. It is required to introduce backlight units into the LCDs for illumination because the liquid crystal molecules are non-illumination materials. Therefore the backlight unit is the most importance element for manufacturing the LCD devices, and the performance thereof is closely related to the displaying effect of the LCD.

Refer to FIG. **1**, the typical backlight unit **10** applied to the LCDs comprises a lightguide plate **100**, optical films **102**, a reflector sheet **104**, a tubular lamp **106**, a frame **108** and a backbezel **110**. The frame **108** and the bezel **110** are assembled together to contain and fabricate above components. When the backlight unit **10** is assembled, the reflector sheet **104** is disposed on the bezel **110**, and then the lightguide plate **100** and the optical films **102** are disposed in sequence on the reflector sheet **104**. Next, the frame **108** is mounted and fastened onto the bezel **110**. And the tubular lamp **106** is inserted into the backlight unit **10** through an opening at the corner of the frame **108**. The tubular lamp **106** is inserted into the slot between the lightguide plate **100** and one edge of bezel **110**.

It is noted that for the purpose of fastening the frame **108** onto the bezel **110** as shown in FIG. **1**, some hooks **110***a* are formed to protrude outwardly from the outside of the sidewalls of the bezel **110**, and correspondingly on the sidewalls of the frame **108** some holes **108***a* are formed. Thus, when the frame **108** is mounted on the bezel **110**, the hooks **110***a* of the bezel **110** are inserted and engaged in the holes **108***a* of the frame **108** for fastening the frame **108** and the bezel **110**. Please refer to FIG. **2**, the assembling structure of the frame **108** and the bezel **110** is illustrated.

Except the aforementioned assembling manner, in some backlight unit, as shown in FIG. **3**, on the sidewalls of the bezel **111** are formed some holes **111***b*, and correspondingly on edges of the frame **109** some hooks **109***b* are fabricated. Therefore, when the frame **109** is disposed onto the bezel **111**, the outside surfaces of the edges of the frame **109** are enclosed and attached by the inside surfaces of the sidewalls of the bezel **111**, and the hooks **109***b* of the frame **109** are inserted and engaged in the respective holes **111***b* of the bezel **111** for fastening the frame **108** and the bezel **111**.

In general, when the assembling manner shown in FIG. **2** is introduced, the edges of the frame **108** are mounted on the outside of the sidewalls of the bezel **110**. It is noted that because the frame **108** made of resin material is flexible and elastic, the operator can disassemble the frame **108** from the bezel **110** easily just by pressing back slightly the hooks **110***a* of the bezel **110** and simultaneously pulling the edges of the frame **108**. Even though such assembling manner has the advantage of easy disassembling, however, the structure strength of the backlight unit is worse due to the resin frame **108** is pliable.

Besides, when the assembling manner shown in FIG. **3** is used, the edges of the frame **109** are enclosed and attached by the inside surfaces of the sidewalls of the bezel **111**. Because the edge of the frame **109** is wedged between the bezel **111** and the lightguide plate **100**, the structure strength of such backlight unit is reinforced. However, due to the bezel **111** made of metal material is too hard, it is difficult to disassemble the frame **109** from the bezel **111**. The operators have to exert themselves to reject the hooks back and extract the frame **109** from the bezel **111**. Apparently, such assembling design will increase the degree of difficulty in reassembling procedures. Under these conditions, the manufacturers usually have to trade off between structure strength and disassembling convenience. And apparently there is a requirement to figure out a new mounting manner for obtaining above two advantages both.

SUMMARY OF THE INVENTION

The prime objective of the present invention is to provide a new assembling manner of the backlight unit for obtaining the both advantages of disassembling convenience and increasing structure strength.

The present invention discloses an assembling structure of a backlight module. The assembling structure comprises following components. A rectangular frame has a long edge and a short edge, wherein first hooks are formed and protruding outwardly on outside surfaces of said long edge, and first holes are formed on said short edge. A rectangular bezel has a long sidewall and a short sidewall, wherein second holes are formed on said long sidewall and second hooks are formed and protruding outwardly on outside surfaces of said short sidewall. When said rectangular frame is mounted onto said rectangular bezel, said long edge is attached to inside surfaces of said long sidewall and said first hooks are inserted and engaged in said second holes for fastening said rectangular frame and said rectangular bezel, and simultaneously said short edge is attached to said outside surfaces of said short sidewall and said second hooks are inserted and engaged in said first holes for fastening said rectangular frame and said rectangular bezel.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIG. **1** illustrates the assembling manner of the components of the backlight unit;

FIGS. **2** & **3** illustrates the conventional assembling manner of the backlight unit;

FIG. **4** illustrates the frame and the bezel fabricated according to the present invention; and

FIG. **5** illustrates the mounting manner of the frame and the bezel according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

As aforementioned, the assembling structure **20** is introduced to contain and fabricate various components of the backlight unit, such as a lightguide plate **302**, optical films **300**, a reflector sheet **304**, a tubular lamp **306** and etc. The assembling structure **20** comprises a frame **200** and a bezel **210**. The frame **200** has a rectangular shape composed of two long edges **202** and two short edges **204**. On each long edge **202** a plurality of holes **206** are formed. And on outer surfaces of each short edge **204** a plurality of hooks **208** are fabricated.

Correspondingly, the bezel **210** also has a rectangular shape. As shown in the FIGURE, the bezel **210** has a rectangular board **212**, two long sidewalls **214** and two short sidewalls **216** which are erect from the edges of the rectangular board **212** respectively. On outer surfaces of each long sidewall **214** a plurality of hooks **218** are formed and protruding outwardly. And on each short sidewall **216** a plurality of holes **220** are formed.

As aforementioned, when the components of the backlight unit are assembled, the reflector sheet **304**, the lightguide plate **302** and optical films **300** are disposed in sequence onto the rectangular board **212** of the bezel **210**. As shown in FIG. **4**, the reflector sheet **304** is disposed on the rectangular board **212** of the bezel **210**, the lightguide plate **302** is disposed on the reflector sheet **304**, and the optical films **300** are disposed on the lightguide plate **302**. Then, the frame **200** is mounted onto the bezel **210** to contain those components. The long edges **202** of the frame **200** are disposed and attached onto the outside surfaces of the long sidewalls **214** of the bezel **210**. Namely, the long sidewall **214** is covered by the edge **202**. And the hooks **218** on the outer surfaces of the long sidewall **214** are inserted and engaged in the holes **206** of the long edge **202** to fasten the frame **200** onto the bezel **210**. In the mean time, the short edge **204** is disposed and attached onto the inside surfaces of the short sidewall **216** of the bezel **210**, and the hooks **208** on the outside surfaces of the short edge **204** are inserted and engaged in the holes **220** of the short sidewall **216** to fasten the frame **200** and the bezel **210**, as shown in FIG. **5**.

It is noted that in most applications of the backlight module the frame **200** is made of flexible materials such as resin, and the bezel **210** is made of metal materials such as aluminum. Therefore, the short sidewalls **216** of the bezel **210** covering the outside of the short edge **200** of the short sidewall **216** can reinforce the structure strength of the backlight unit. AT the same time, because the long edges **202** of the frame **200** are attached to the outside of the long sidewalls **214** of the bezel **210**, the frame **200** can be disassembled from the bezel **210** very easily by pressing slightly the hooks **218** of the bezel **210** and pulling the long edges **202** of the frame **200**.

it is noted that in the above embodiment, the long edges **202** of the frame **200** are formed with the holes **206**, and the short edges **204** are formed with hooks **218**. However, in another embodiment, other mounting manners can be chosen according to the requirements of designing backlight units. For example, the short edges of the frame can be defined with holes, and the long edges of the frame can be fabricated with protruding hooks. Correspondingly, the short sidewalls of the bezel are fabricated with hooks and the long sidewalls thereof are drilled to have holes thereon. Thus, the assembling structure with the frame mounted onto the bezel can have both the advantages of enhancing structure strength and easy disassembling.

Besides, in a further embodiment, only one edge of the rectangular frame is fabricated with holes and the others (the three edges) are fabricated with protruding hooks. Certainly, in this design, only one sidewall of the bezel is fabricated with hooks, and the others are fabricated with holes for fastening the frame and the bezel.

It is noted that in most backlight units the tubular lamp of the backlight unit is disposed on the inside of one long sidewall of the bezel. So in a preferred embodiment the long edges of the frame are disposed to attach the outside surfaces of the long sidewalls of the bezel. Therefore, the long sidewall of the bezel is more closely to the tubular lamp and can have efficient heat dissipations due to the metal material of the bezel. And that can prevent the overheat issues of the tubular lamp in the prior art. In other words, the long sidewall adjacent to the tubular lamp is fabricated with hooks that are protruding outwardly from the outside surfaces of the long sidewall. And on the corresponding long edges of the frame the holes are formed for receiving and wedging the hooks of the bezel, in order to fasten the frame and the bezel and to let the sidewall of the metal bezel more closely to the tubular lamp.

Except the design of assembling the frame and the bezel as illustrated in the above embodiment, the fastening manner can also be applied to the assembling structure of two frames. For example, some first hooks are fabricated on the outside of the first edge of an upper frame, and on the second edges of the upper frame some first holes are formed. In the mean time, on the third edges of a lower frame some second holes are formed to receive and wedge the first hooks, and outside the fourth edges of the lower frame some second hooks are fabricated to insert and engage the first holes for fastening the upper and lower frames.

The assembling structures provided in the present invention have many advantages. Because the two long edges of the frame are disposed to mount and cover the two long sidewalls of the bezel, and the two short edges of the frame are disposed inside the two short sidewalls of the bezel. So the assembling structures can obtain both the reinforced structure strengths and the disassembling convenience.

As is understood by a person skilled in the art, the foregoing preferred embodiment of the present invention is illustrated of the present invention rather than limiting of the present invention. It is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar design.

What is claimed is:

1. An assembling structure of a backlight module for containing and fabricating components of said backlight module, said assembling structure comprising:

a frame, having a first edge and a second edge, wherein on outer surfaces of said first edge a plurality of first hooks are formed to protrude outwardly, and on outer surfaces of said second edge a plurality of first holes are formed;

a bezel, made of metal material, having a first sidewall and a second sidewall, wherein on said first sidewall a plurality of second holes are formed, and on outer surfaces of said second sidewall a plurality of second hooks are formed to protrude outwardly;

wherein said first edge is disposed onto inside surfaces of said first sidewall, said first hooks are inserted and engaged in said second holes, said second edge is disposed onto outside surfaces of said second sidewall, and said second hooks are inserted and engaged in said first holes as said frame is mounted onto said bezel.

2. The assembling structure of claim 1, wherein said frame is made of resin material.

3. The assembling structure of claim 1, wherein a tubular lamp of said backlight module is disposed inside and adjacent to said second sidewall of said bezel.

4. The assembling structure of claim 1, wherein said frame has a rectangular shape, and said first edge of said frame is a short edge, and said second edge of said frame is a long edge.

5. The assembling structure of claim 1, wherein said bezel has a rectangular board, and said first sidewall and said second sidewall are erect from edges of said rectangular board, said first sidewall is a short sidewall of said bezel and said second sidewall is a long sidewall thereof.

6. An assembling structure of a backlight module for containing and assembling components of said backlight module, said assembling structure comprising:

an upper frame, made of resin material, having a first edge and a second edge, wherein on outside surfaces of said first edge first hooks are formed to protrude outwardly, and on said second edge first holes are formed; and

a lower frame, made of metal material, having a third edge and a fourth edge, wherein on said third edge second holes are formed, and on outside surfaces of said forth edge second hooks are formed to protrude outwardly;

wherein said first edge is disposed inside said third edge and said first hooks are inserted and engaged in said second holes, said second edge is attached to the outside surfaces of said fourth edge, and said second hooks are inserted and engaged in said first holes as the upper frame is mounted onto the lower frame.

7. The assembling structure of claim 6, wherein a tubular lamp of said backlight module is disposed inside said fourth edge of said lower frame.

8. A backlight unit comprising:

a bezel made of metal material, having a first sidewall and a second sidewall, wherein on said first sidewall a plurality of first holes are formed, and on outer surfaces of said second sidewall a plurality of first hooks are formed to protrude outwardly;

a lightguide plate, disposed above said bezel;

a frame, disposed above said lightguide plate and mounted onto said bezel, having a first edge and a second edge, wherein on outer surfaces of said first edge a plurality of second hooks are formed to protrude outwardly, and on outer surfaces of said second edge a plurality of second holes are formed, wherein said first edge is disposed onto inside surfaces of said first sidewall, and said second hooks are inserted and engaged in said first holes for fastening said frame and said bezel, simultaneously said second edge is disposed onto outside surfaces of said second sidewall, and said first hooks are inserted and engaged in said second holes for fastening said frame and said bezel; and

a tubular lamp, disposed on said bezel, beside said lightguide plate, and adjacent to inside surfaces of said second sidewall of said bezel.

9. The backlight unit of claim 8, wherein said frame is made of resin material.

10. The backlight unit of claim 8, further comprising a reflector sheet, disposed on said bezel and beneath said lightguide plate.

11. The backlight unit of claim 8, further comprising optical films, disposed on said lightguide plate and under said frame.

12. The backlight unit of claim 8, wherein said frame has a rectangular shape, and said first edge of said frame is a short edge, and said second edge of said frame is a long edge.

13. The backlight unit of claim 12, wherein said bezel has a rectangular board, and said first sidewall and said second sidewall are erect from edges of said rectangular board, said first sidewall is a short sidewall of said bezel and said second sidewall is a long sidewall thereof.

* * * * *

EXHIBIT E

US006778160B2

(12) **United States Patent**
Kubota et al.

(10) **Patent No.: US 6,778,160 B2**
(45) **Date of Patent: Aug. 17, 2004**

(54) **LIQUID-CRYSTAL DISPLAY, LIQUID-CRYSTAL CONTROL CIRCUIT, FLICKER INHIBITION METHOD, AND LIQUID-CRYSTAL DRIVING METHOD**

(75) Inventors: **Tetsu Kubota**, Fujisawa (JP); **Akihiro Funakoshi**, Kamakura (JP); **Takuya Ishikawa**, Hino (JP)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 218 days.

(21) Appl. No.: **09/760,131**

(22) Filed: **Jan. 12, 2001**

(65) **Prior Publication Data**

US 2001/0024181 A1 Sep. 27, 2001

(30) **Foreign Application Priority Data**

Jan. 17, 2000 (JP) 2000-007816

(51) **Int. Cl.**[7] **G09G 3/36**

(52) **U.S. Cl.** **345/89**; 345/98; 345/77; 345/88; 345/690

(58) **Field of Search** 345/88, 63, 89, 345/77, 90, 87, 611, 690, 147, 148, 211, 102, 212

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JP	07-056532	3/1995
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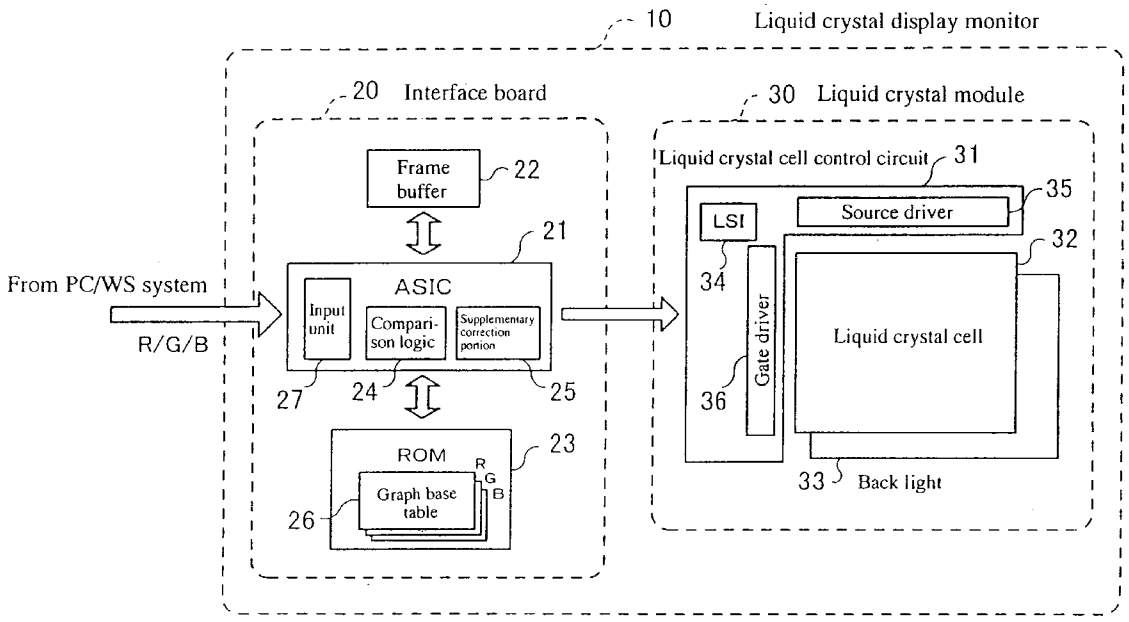
Primary Examiner—Regina Liang
Assistant Examiner—Jennifer T. Nguyen
(74) *Attorney, Agent, or Firm*—Derek S. Jennings; David Aker

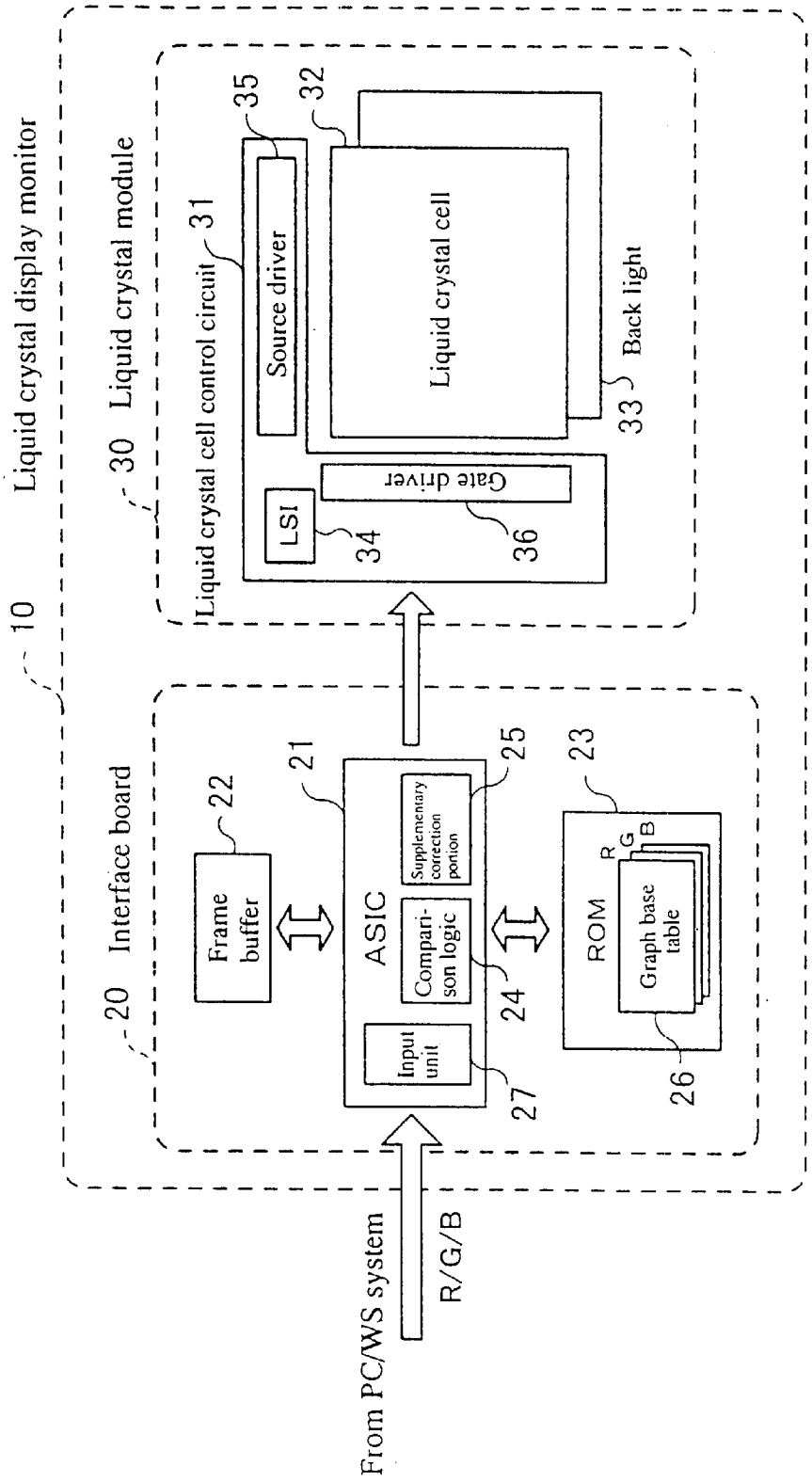
(57) **ABSTRACT**

A liquid crystal display comprises an input for inputting a video signal from a host and a storage medium for storing the previous brightness level of the video signal input through the input. A determinator is provided for determining an output brightness level based on the previous brightness level stored in the storage medium and the next brightness level of the next video signal input to the input, so as to make the time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level. Further included are drivers for driving an image displaying liquid crystal cell based on the output brightness level determined by the determinator.

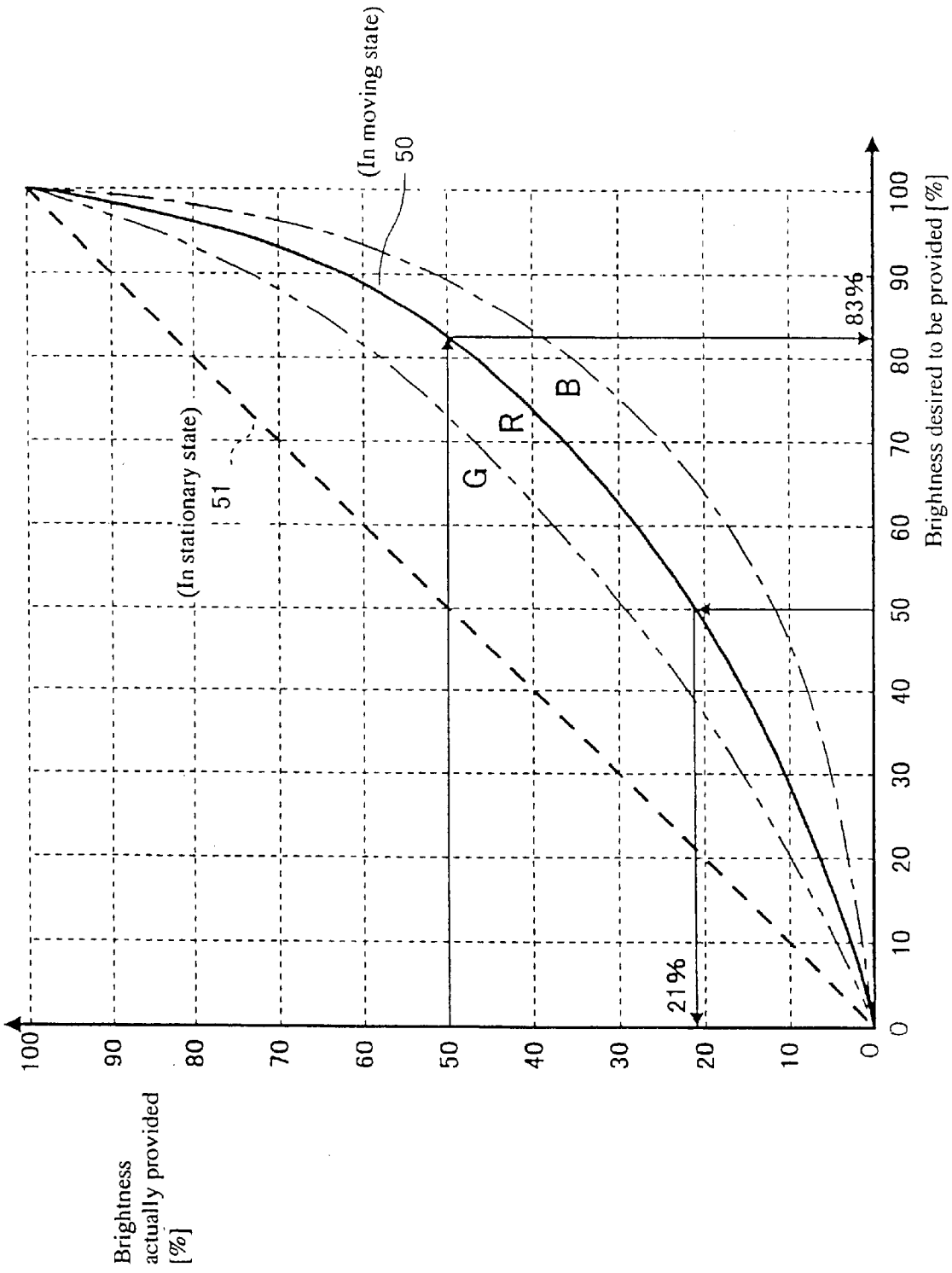
14 Claims, 11 Drawing Sheets



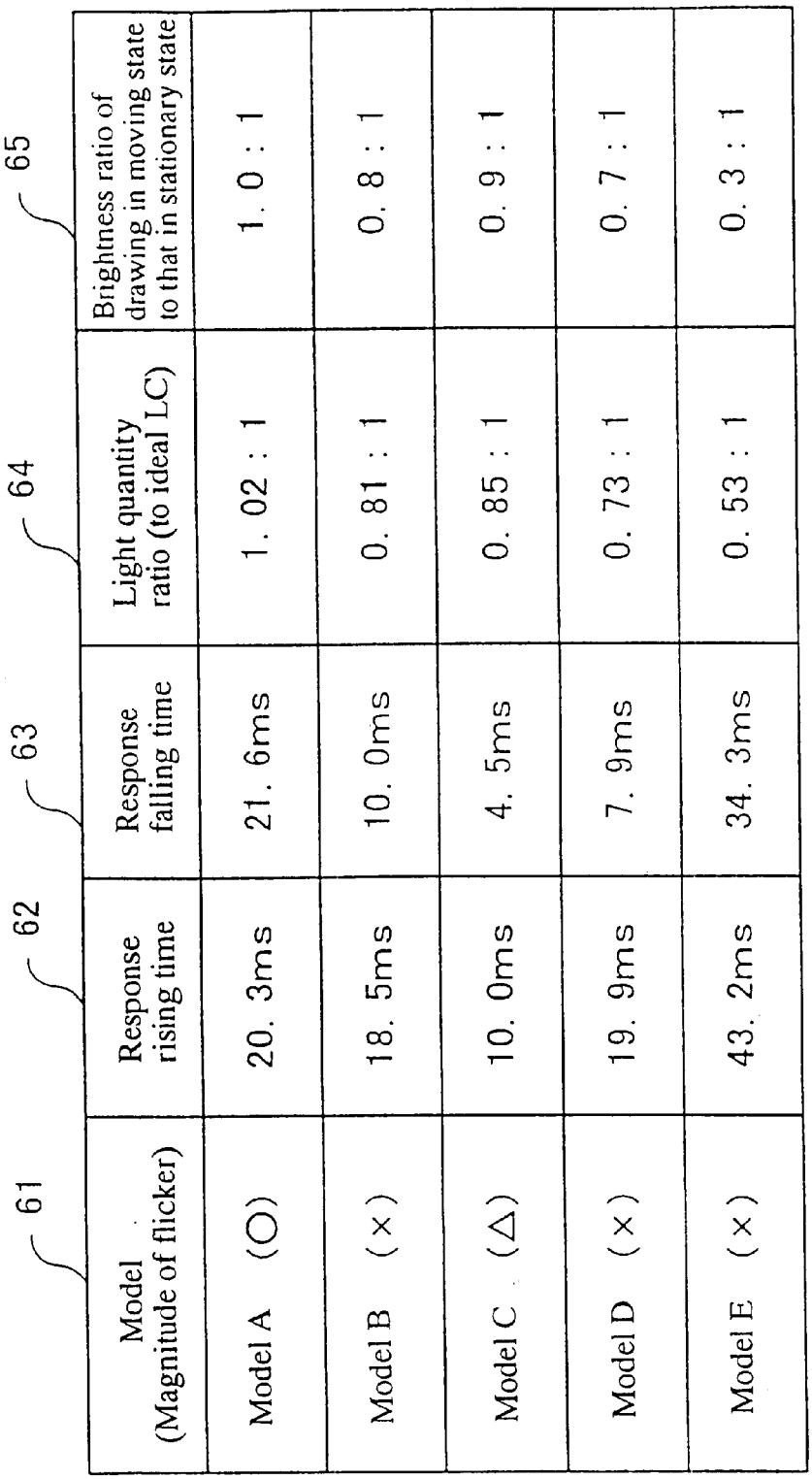
[Figure 1]


Liquid crystal display monitor
10
Liquid crystal module
30
Liquid crystal cell control circuit
31
Source driver
35
32
Liquid crystal cell
Back light
33
Gate driver
LSI
34
36
Interface board
20
Frame buffer
22
21
ASIC
Supplementary correction portion
25
Compari-son logic
24
Input unit
27
23
ROM
R
G
B
Graph base table
26
From PC/WS system
R/G/B

[Figure 2]

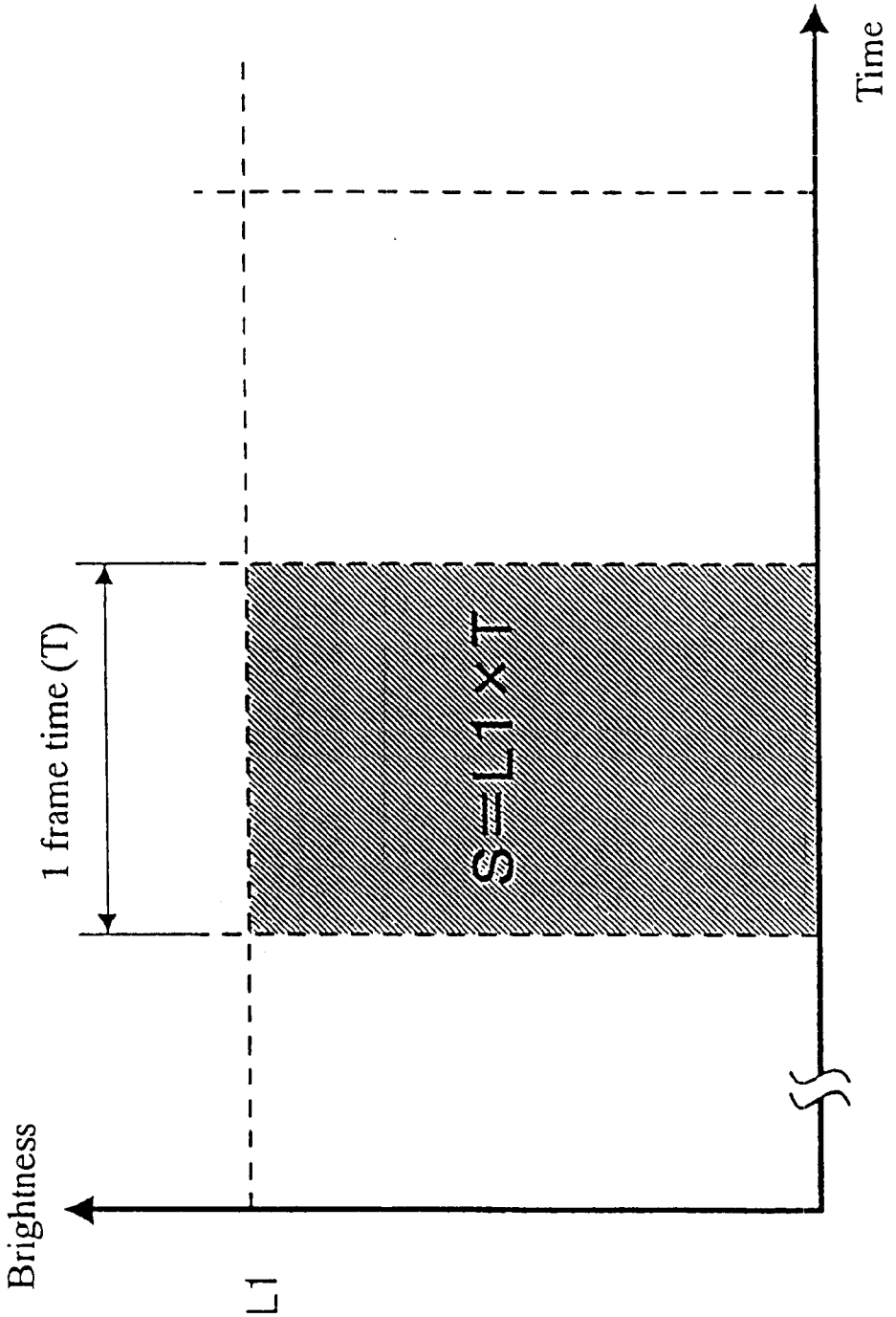

(In moving state)
50
(In stationary state)
51
G
R
B
83%
21%
Brightness desired to be provided [%]
Brightness actually provided [%]
0
10
20
30
40
50
60
70
80
90
100

[Figure 3]

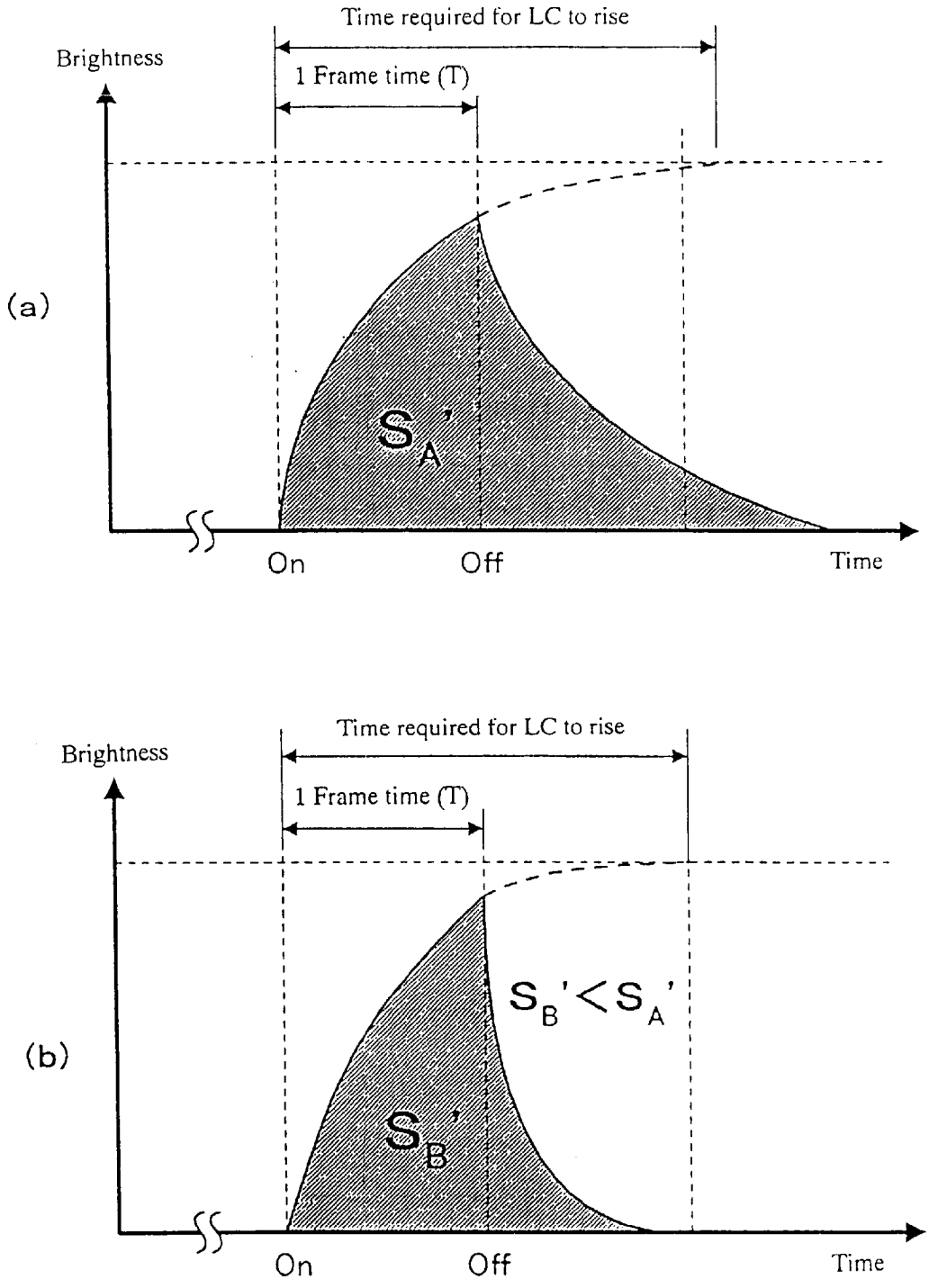


61 Model (Magnitude of flicker)	62 Response rising time	63 Response falling time	64 Light quantity ratio (to ideal LC)	65 Brightness ratio of drawing in moving state to that in stationary state
Model A (○)	20.3ms	21.6ms	1.02 : 1	1.0 : 1
Model B (×)	18.5ms	10.0ms	0.81 : 1	0.8 : 1
Model C (△)	10.0ms	4.5ms	0.85 : 1	0.9 : 1
Model D (×)	19.9ms	7.9ms	0.73 : 1	0.7 : 1
Model E (×)	43.2ms	34.3ms	0.53 : 1	0.3 : 1

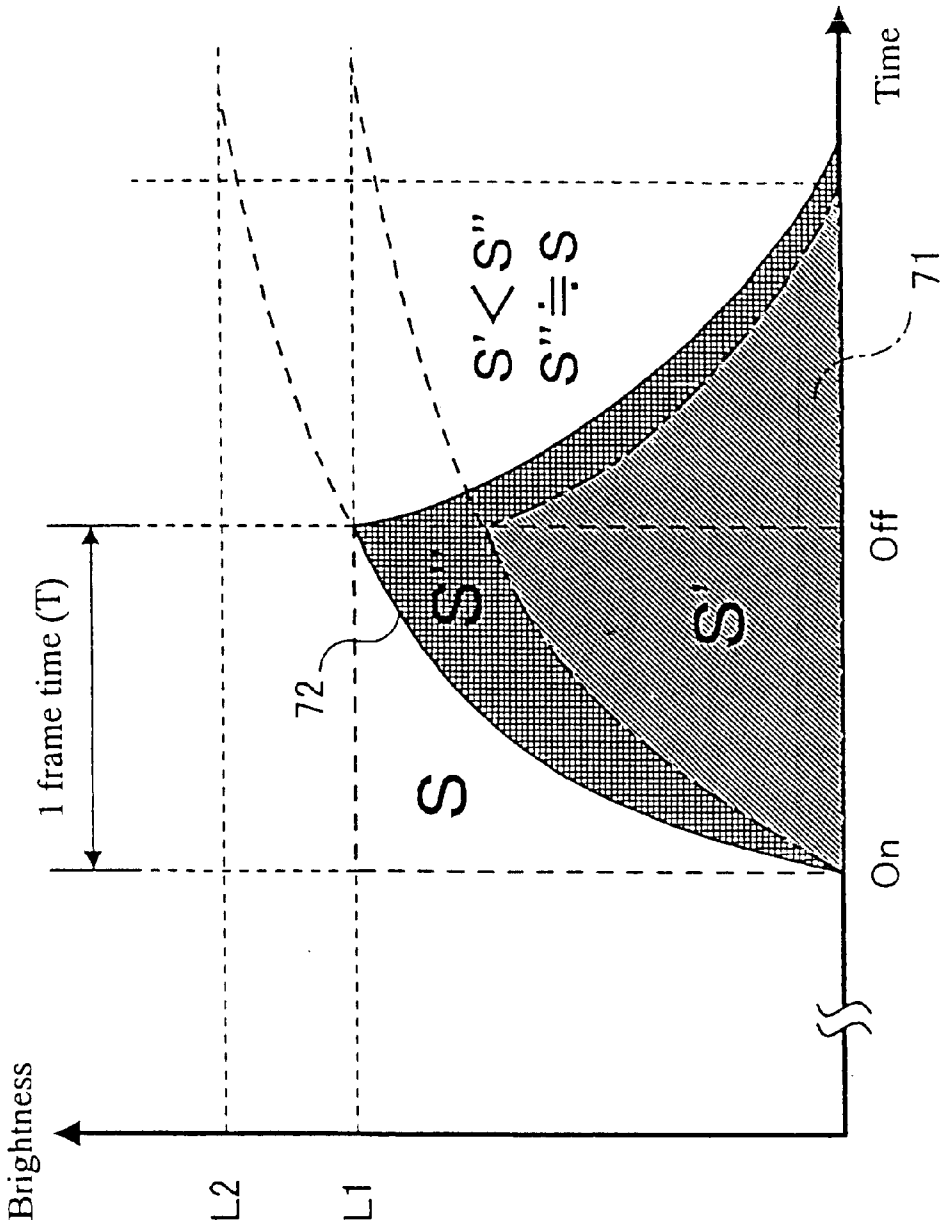
[Figure 4]



[Figure 5]


Time required for LC to rise
Brightness
1 Frame time (T)
(a)
S_A'
On
Off
Time
Time required for LC to rise
Brightness
1 Frame time (T)
$S_B' < S_A'$
(b)
S_B'
On
Off
Time

[Figure 6]

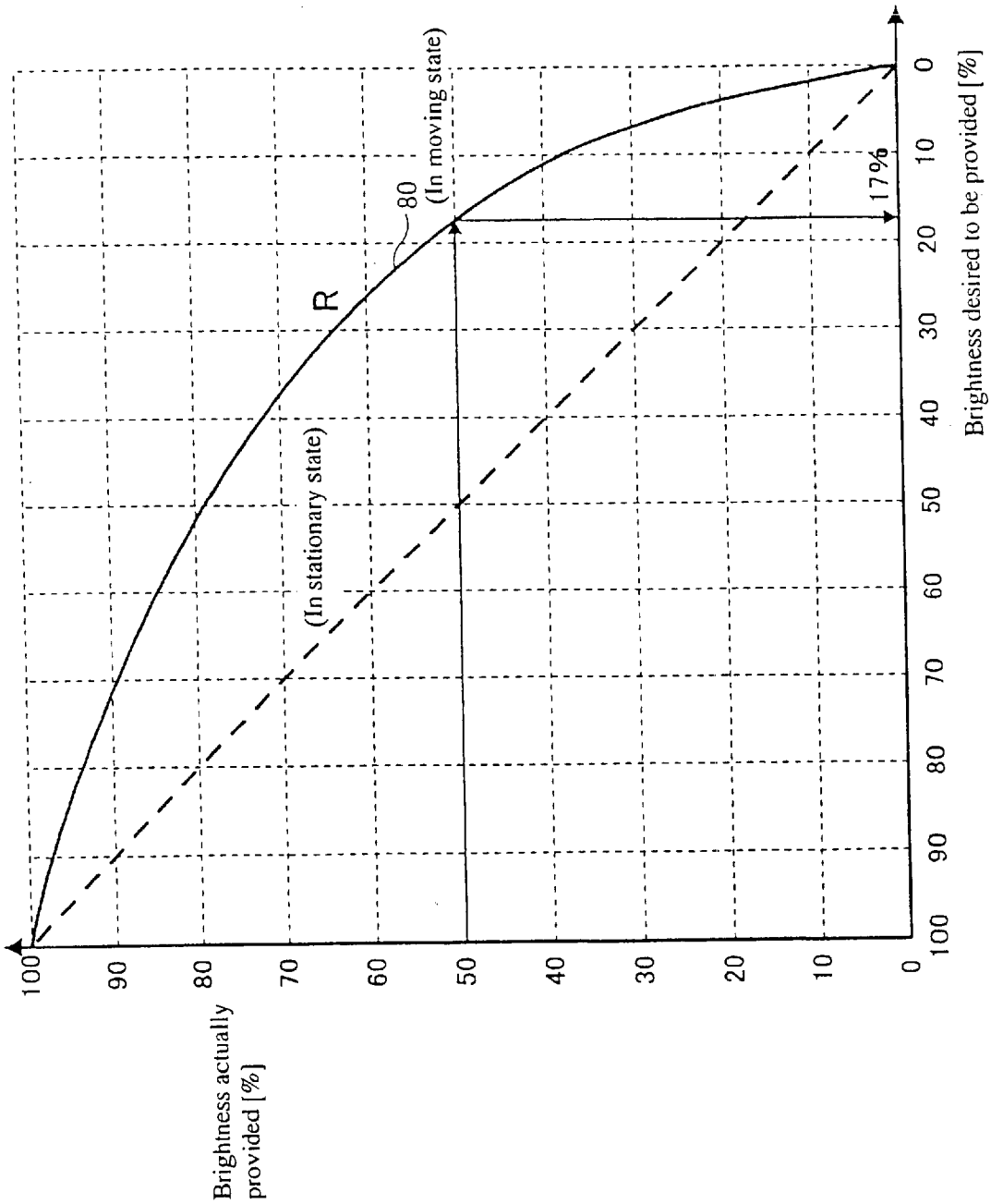


[Figure 7]

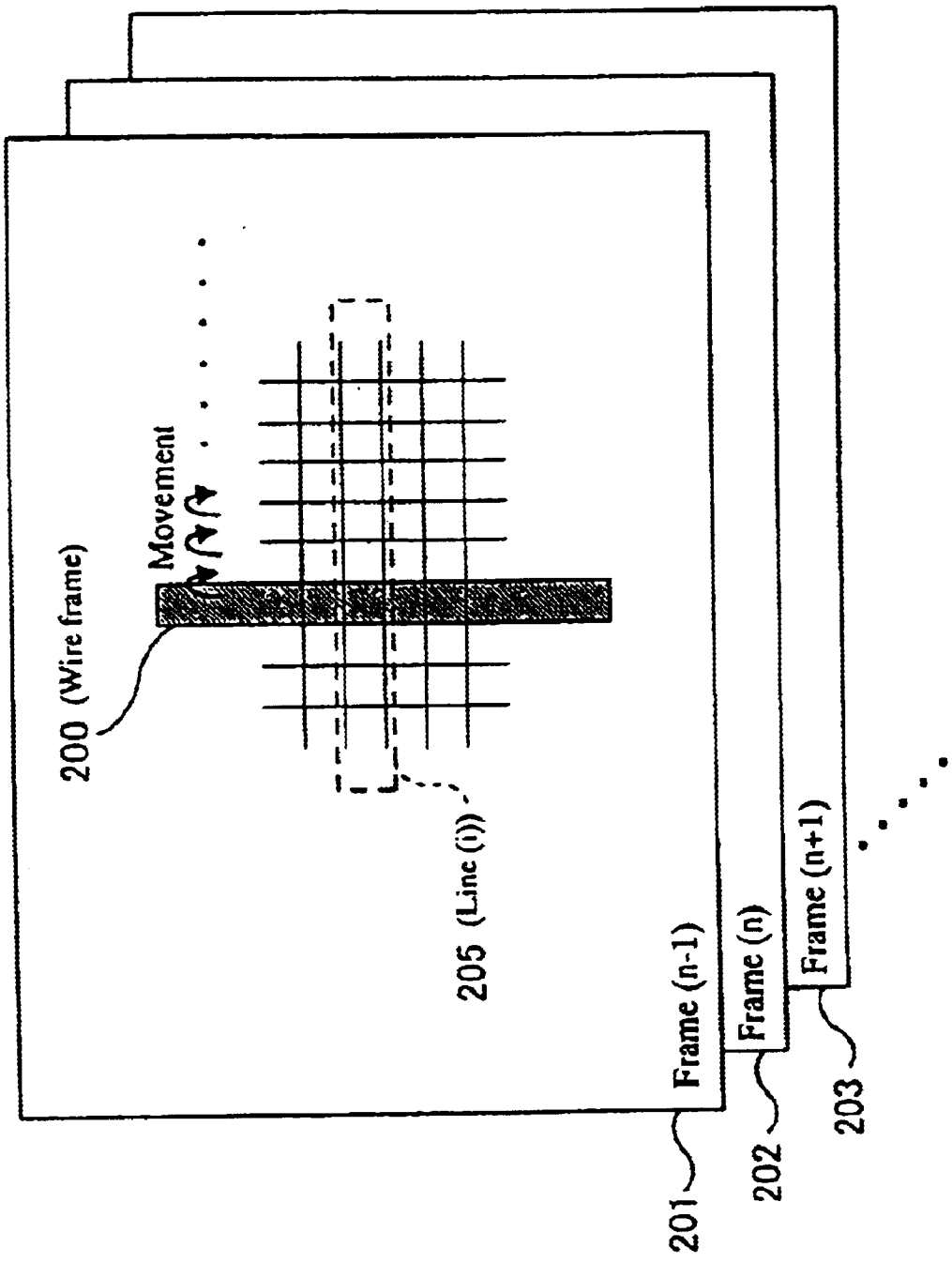
26 (Graph base table)

Previous brightness \ Next brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

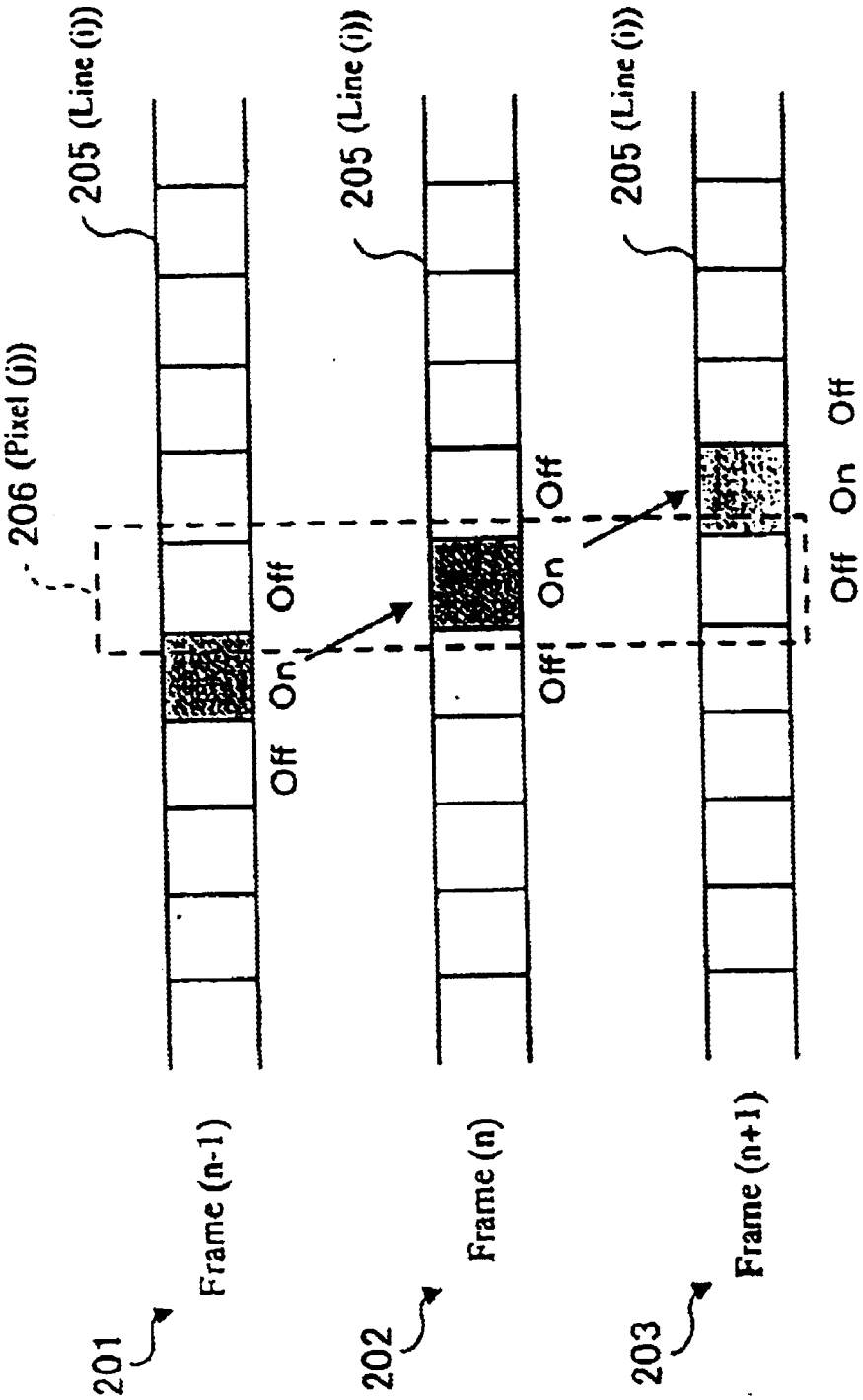
[Figure 8]


Brightness actually provided [%]
100
90
80
70
60
50
40
30
20
10
0
Brightness desired to be provided [%]
0
10
20
30
40
50
60
70
80
90
100
17%
80
(In moving state)
R
(In stationary state)

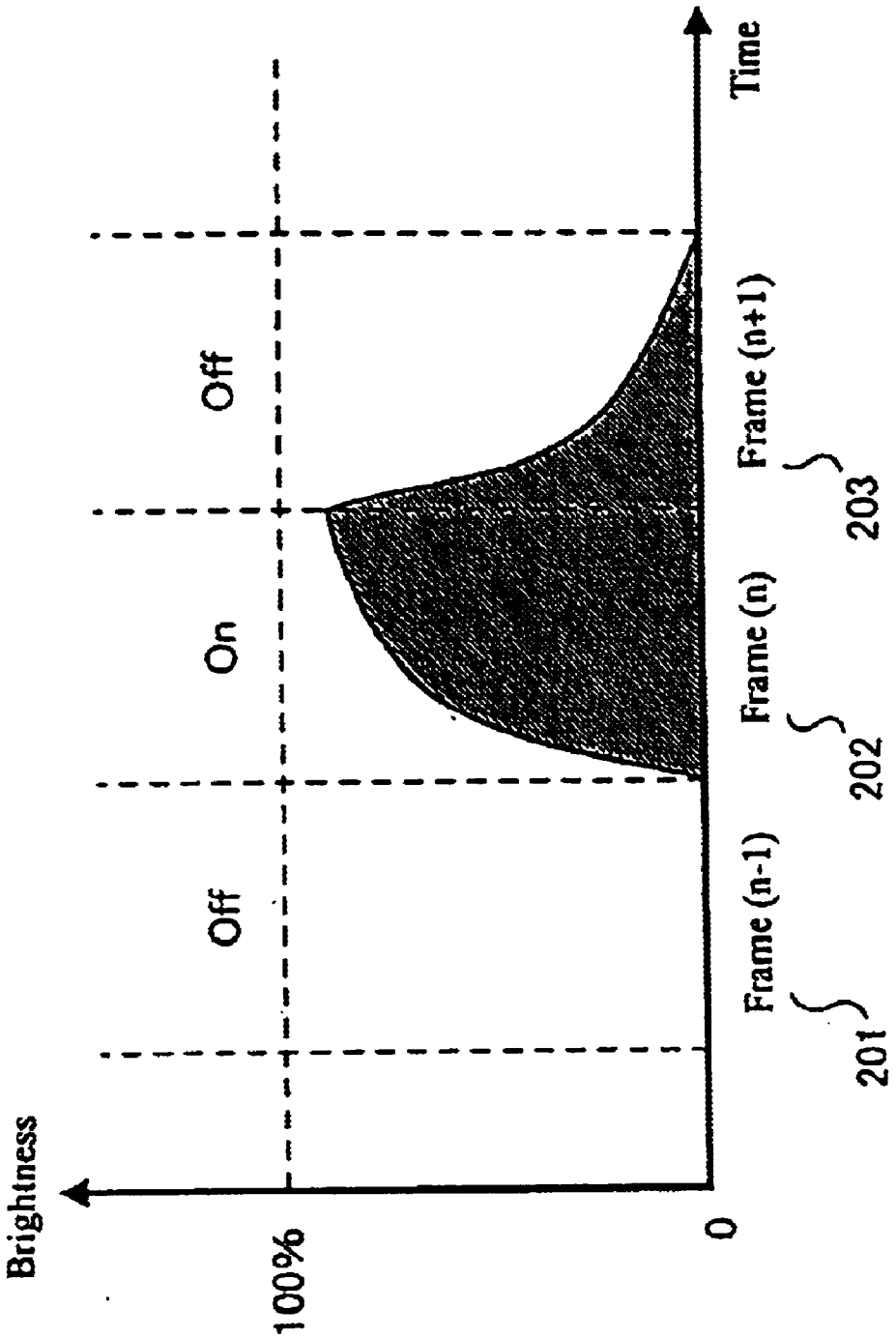
[Figure 9] PRIOR ART



[Figure 10] PRIOR ART



[Figure 11] PRIOR ART



LIQUID-CRYSTAL DISPLAY, LIQUID-CRYSTAL CONTROL CIRCUIT, FLICKER INHIBITION METHOD, AND LIQUID-CRYSTAL DRIVING METHOD

FIELD OF THE INVENTION

The present invention relates to a method for compensating poor response time, and in particular, to a method and an apparatus for inhibiting flicker resulting from the poor response time of a liquid crystal display.

BACKGROUND OF THE INVENTION

In recent years, besides cathode ray tubes (CRTs), liquid crystal displays (LCDs) have come into widespread use as display devices for various types of image displays and monitors for units such as personal computers (PCs) and television sets. The LCDs can be made significantly smaller and lighter than CRTs. In addition, many improvements in the display performance of LCDs, including low geometric distortion as well as considerably high picture quality, have been achieved. For these reasons, the LCDs have gained the spotlight as a mainstream display device used in video equipment of the future.

However, because of the poor response characteristic of the liquid crystal itself, the LCDs has the potential problem of poor response time. That is, in a typical display device used in the industry, the display is refreshed at a frame rate of 60 frames per minute, or, every (1÷60=) 16.7 ms. On the other hand, the response time of liquid crystals used in many current LCDs required to change from black to white is 10 to 50 ms, typically 20 to 30 ms. This means that one frame time in the display is shorter than the response time of most liquid crystals. As a result, problems, such as the visual persistence of moving images and inability to keep up with fast-moving images, caused by the response delay of the LCDs have become obvious.

The term "response time" used in the industry refers to the sum of (1) time required to reverse color by applying a voltage to a liquid crystal cell and (2) time required to restore the original color by the removal of the applied voltage. The term "frame" used in the industry represents the scanning of all the images (picture elements) that should form one complete picture on the display.

Some solutions to these poor response time problems with the LCD are disclosed in, for example, Published Unexamined Japanese Patent Applications Nos. 2-153687, 4-365094, 6-62355, and 7-56532.

In Published Unexamined Japanese Patent Application No. 2-153687, a LCD is provided which is configured to discriminate between a static image area having less motion and a fast-moving area and apply a signal process only to the moving area to emphasize time-based changes in an image, thereby improving response time in the image area where better response time is required to reduce visual persistence and noise.

In Published Unexamined Japanese Patent Application No. 4-365094, a LCD is provided which is configured to be driven by reading pre-stored optimum image data according to the direction and degree of a change when the image data changes, thereby allowing the LCD to rapidly follow the fast-changing image.

In Published Unexamined Japanese Patent Application No. 6-62355, a technology is disclosed which superposes a difference component between fields or frames on a video signal to provide pulse stepping drive when the video signal changes between the fields or frames, thereby improving the response of display elements in an LCD.

In Published Unexamined Japanese Patent Application No. 7-56532, a technology is disclosed which provides table memory containing a table of image increase/decrease values and drive a liquid crystal panel (liquid crystal cell) by performing an addition/subtraction in order to improve response changes due to changes in the gray scale in the liquid crystal panel. However, the amount to be added or subtracted is expressed only by the word "optimum" and no specific amount is disclosed.

One problem associated with picture quality in LCDs which do not arise in a CRT display is flicker. When, for example, a wire-frame model in a CAD application is displayed on the LCD and the operator (user) moves it continuously at a relatively low speed, about several tens pixels per minute, the entire wire-frame model appears to blink in a cycle of several to several tens Hz. This effect is called flicker. While this effect does not occur in CRT displays, it occurs in most existing types of LCDs and many customers have requested minimization of the flicker urgingly. The flicker herein differs in symptom and cause from that in CRT displays which is caused by infrequent refresh.

In CAD applications, a wire-frame model is typically displayed using many thin lines in white or other colors against a black background. Assuming that the wire-model is white (all of the colors R (read)/G (green)/B (blue) are "ON") as an example, no problem arises when the model stay stationary on the screen because only a few frames are required to achieve an proper brightness. However, if the operator move the model on the screen, the proper brightness cannot completely be achieved. That is, if a pixel is made light up only in one frame, the brightness of the pixel may not reach the predetermined brightness because the response of the LCD itself is slow as mentioned above. This situation will be described below with reference to the drawings.

FIG. **9** shows the movement of lines when a wire-frame model is moved on the screen. FIG. **10** shows on/off states of the pixels on line (i) in each frame at the time point in FIG. **9**. FIG. **11** shows a change in the brightness of pixel (j).

Herein, as shown in FIG. **9**, in the case where attention is paid to a particular pixel, assuming that a line of the wire frame **200** moves through frames (n−1) **201** to (n) **202** to (n+1) **203** in sequence. That is, the pixel lights up in a time period equivalent to the frames in which the line passes over the pixel and goes off immediately after that.

Focusing attention on line (i) **205** represented by a dashed line, in particular, on the particular pixel, each frame is driven from OFF to ON by the movement of pixel (j) **206**, then one frame after goes back from ON to OFF, as shown in FIG. **10**. However, because the response time of commonly-used liquid crystals is longer than 16.7 ms, pixel (j) **206** changes back to black before completely returning from black to white. That is, as shown in FIG. **11**, pixel (j) **206** is OFF in frame (n−1) **201**, goes ON in frame (n) **202**, then goes OFF in frame (n+1) **203**. However, the target brightness of pixel (j) **206** is not reached even though it is turned on in order to achieve 100% brightness in frame (n) **202**. As a result, the brightness of the line drawing during movement will be low. The inventors have found that when a wire-frame model is continuously moved in a CAD application, the wire-frame model in fact repeatedly alternates between moving and stationary states every several frames and blinks due to a difference in display brightness

between the moving and stationary states, and this difference causes "flicker."

Many manufacturers have actively sought after a method for improving the response of LCD panels by improving a liquid crystal material itself or narrowing the gap between glass plates in order to reduce flicker of LCDs. Some state-of-the-art products on the market have an improved response time of about 25 ms including rising and falling time. Another LCD technologies for reducing response time to several ms have been disclosed in some academic conferences. However, these approaches to improve an LCD panel itself can hardly to provide mass-production products because of their low reliability, and there are many other problems to be solved to put them into practical use.

In view of these technical problems, it is a primal object of the present invention to inhibit the flicker effect as visual perception by the panel driving circuitry which drives an LCD.

It is another object of the present invention to drive the LCD by applying an offset to a moving model without globally determining whether the model is moving or stationary.

SUMMARY OF THE INVENTION

To achieve above-mentioned objects, a feature of the present invention includes a liquid crystal display comprises an input for inputting a video signal from a host and a storage medium for storing the previous brightness level of the video signal input through the input. A determinator is provided for determining an output brightness level based on the previous brightness level stored in the storage medium and the next brightness level of the next video signal input to the input, so as to make the time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level. Further included are drivers for driving an image displaying liquid crystal cell based on the output brightness level determined by the determinator.

Another feature of the present invention includes a liquid crystal display characterized by comprising a driver for driving each of the pixels forming an image for each frame to a liquid crystal cell displaying the image, an input for inputting an moving-state video signal which changes from the off state to the on state on transition to a particular frame in the frames and returns to the off state after the particular frame is completed, and elements for setting an offset for making the quantity of light closer to the quantity of light in a stationary state in which the moving-state video signal is continuously turned on for the particular frame. The liquid crystal display further includes a generator for applying the offset set by the setting elements to the moving-state video signal input through the input means to generate an output video signal, and an output for outputting the output video signal generated by the generation means to the drive means. By configuring the apparatus in this way, a difference in brightness between a stationary state and a moving state which can be considered as the principal cause of flicker can be reduced to inhibit visually perceptible flicker.

Yet another feature of the present invention is further characterized by a liquid crystal control circuit having a function for inhibiting flicker caused by a difference in brightness when an input wire-frame model is displayed by liquid crystal cells. The liquid crystal control circuit includes a storage portion for storing an offset in brightness in a moving state in which the wire-frame model having a predetermined gray scale changes from frame to frame with respect to a particular pixel. This is with relation to brightness output in a stationary state in which the wire-frame model having the predetermined gray scale is displayed on the particular pixel across a plurality of frames. Further included is a correction portion for applying the offset stored in the storage portion to the gray scale of the wire-frame model if the input wire-frame model is in a moving state.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram for showing the overall configuration of a liquid crystal display (LCD) apparatus according to one embodiment of the present invention.

FIG. **2** is a graph showing an example of brightness of a wire-frame image in a moving state on the LCD used with the embodiment.

FIG. **3** is a table showing the measurements of response time at the maximum brightness of a liquid crystal used in five LCD models (model A to E).

FIG. **4** shows the response characteristic of an ideal liquid crystal.

FIGS. **5** (*a*) and (*b*) are graph showing the response characteristics of models A and B shown in FIG. **3** by brightness versus time when a pixel is turned on for only one frame.

FIG. **6** shows an effect when brightness is set by taking a required offset into consideration.

FIG. **7** shows a relation between brightness L1 and brightness L2 in table form;

FIG. **8** is a graph showing desired brightness versus brightness actually provided when brightness falls.

FIG. **9** shows the movement of a line on the screen when a wire-frame model is moved on the screen.

FIG. **10** shows the ON/OFF states of a pixel on line (i) in each frame.

FIG. **11** shows changes in brightness of pixel (i).

DETAILED DESCRIPTION OF THE INVENTION

The "ideal quantity of light" herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid crystal cells (liquid crystal panels). Quantity of light is considered as a time integration quantity of a brightness change and can be expressed as brightness_time, if the brightness is constant. The representation "substantially equal level" refers to a level which is not completely the same but can be accepted as a substantially equivalent level, and includes a level which is closer to an ideal quantity of light than no preventive measures are taken.

The determinator is characterized by comprising a table for storing a brightness level determined by the characteristic of a liquid crystal cell according to a relation between the previous brightness level and the next brightness level, and determining an output brightness level by modifying the next brightness level based on the brightness level read from the table. With this configuration, flicker due to changes in

the quantity of light during the movement of the model can be inhibited without globally determining whether a model is in a moving or stationary states. In addition, a correction for a "halftone" can be made, thereby allowing a decrease in brightness level, which is remarkable in halftones, to be addressed properly.

The video signal input through the input consists of a plurality of color signals and the table in the determinator is provided for each of the color signals so that a brightness level correction for each color can be made with respect to flicker perception of the human eye to reduce a difference in brightness, thereby an easy-on-the-eye liquid crystal display can be provided to the user. While the color signals may be R (read), G (green), B (blue) signals used in displays, other display systems can also be used.

The offset set by the setting elements can be determined based on a time integration quantity, which is a change in brightness in the moving-state vide signal integrated with respect to time, and the quantity of light in stationary state, thus a difference in brightness can be preferably reduced in consideration of the human visual perception characteristic to inhibit flicker appropriately.

The moving-state video signal passed through the input consists of a plurality of color signals, the offset set by the setting elements is determined for each of the color signals, and the generator generates the output video signal for each color signal based on the offset determined for each color signal. Thus a difference in brightness between moving and stationary states can be corrected for each color signal to inhibit flicker on a color image display.

The apparatus further comprises a frame buffer for storing the brightness information of the input wire-frame model as the previous brightness, and characterized by that the storage portion stores the offset as table information based on a relation between the previous brightness stored in the frame buffer and the brightness of the next input wire-frame model, thus, flicker in a moving state can be advantageously inhibited without providing separate determining units for moving and stationary states.

Because the wire-frame model in the present invention is a model consisting of a large number of thin lines in white or other colors in a CAD application, for example, in which flicker is especially troublesome, the flicker inhibition by correcting gray scale of such a wire-frame model in a moving state is highly effective.

The liquid crystal control circuit may be implemented as an interface board provided in a liquid crystal display monitor. The liquid crystal display monitor may be one used with a desktop personal computer or a CAD computer as well as one integrated with a host, like a notebook computer.

In another category, the present invention is a flicker inhibition method for inhibiting flicker caused by a difference in brightness when an input wire-frame model is displayed by a liquid crystal cell. The method is characterized by storing a relation between brightness in a stationary state in which a wire-frame model having a predetermined gray scale is displayed on a particular pixel across a plurality of frames and brightness in a moving state in which the wire-frame model having the predetermined gray scale changes frame to frame with respect to the particular pixel, applying an offset based on the stored relation to the gray scale of the wire-frame model if the input wire-frame model is in a moving state, and driving the liquid crystal cell based on the gray scale to which the offset is applied to display the wire-frame model.

The moving state brightness used for storing the relation is the brightness when the particular pixel changes back to the off state one frame after it is driven from the off state to the on state during the passage of the wire-frame model over the particular pixel.

Furthermore, the brightness in the moving state which is used when the relation is stored is the quantity of light equal to the brightness change integrated with respect to time.

With this configuration, a difference in the brightness of the wire-frame model between its moving state and stationary state can be reduced to inhibit flicker which would otherwise noticeably occur.

Viewing the present invention as a liquid crystal driving method, the liquid crystal driving method of the present invention is characterized by the steps of storing first brightness information for an input pixel in a frame buffer, and applying, based on second brightness information for the next input pixel and the first brightness information stored in the frame buffer, an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is brightness in a stationary state to the second brightness information. The steps further include the outputting of the second brightness information to which the offset is applied to a driving circuit for driving an liquid crystal cell, and storing the second brightness information for the input pixel in a frame buffer. This liquid crystal driving method allows the inhibition of flicker by using a simple apparatus without globally determining whether a model is moving or stationary.

The present invention is still further characterized in that the input pixel consists of a plurality color signals and includes the step of storing the first brightness information in the frame buffer stores the first brightness information for each of the color signals, and the step of applying the offset applies the offset to each of the color signals, thus the brightness of each color of a color image consisting of a plurality of color signals can be corrected individually, allowing more adequate flicker inhibition.

The offset applying step is characterized by the step of reading a pre-stored offset based on the relation between the first and second brightness information and applying the read offset to the second brightness information.

The brightness information at a moving time that is used in a storage operation based on the relation is the quantity of light equal to a brightness change for each color signal integrated with respect to time, therefore correction according to the human visual perception characteristics can be made to address the problems resulting from human visual perception of flicker more properly.

The present invention will be described below with respect to the embodiments shown in the accompanying drawings.

FIG. **1** is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number **10** denotes a liquid crystal display monitor (LCD monitor) as a liquid crystal display panel, which comprises, for example, a liquid crystal module **30** having a thin-film transistor (TFT) structure and an interface (I/F) board **20** connected to a digital or analog interface to a personal computer (PC) or a workstation (WS) system for supplying a video signal to the liquid crystal module **30**. If a notebook PC is used, a system unit (not shown) is integrated with the liquid crystal display monitor **10**. If a monitor having a display device separated from its system unit is configured, a system unit (not shown) is attached to the LCD monitor **10** to form a liquid crystal display.

The I/F board **20** comprises a input unit **27** for inputting video data from a host such as a PC/WS system, a com-

parison logic **24** for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) **21** including a logic having units such as a supplementary correction portion **25** for performing a supplementary correction. The I/F board **20** also comprises a frame buffer **22** for temporarily storing the input video signal and read-only memory (ROM) **23** containing information needed for the operation of the ASIC **21**. The frame buffer **22** stores input video signal value input previously and provides it to the ASIC **21**. The ROM **23** includes a graph base table **26** which is required for the supplementary correction in the ASIC **21** and is set for each of R/G/B input color signals. The graph base table **26** contains a brightness level to be output based on a relation between the previous brightness and the next brightness in a table form which will be described later.

The liquid crystal module **30** consists of three main blocks a liquid cell control circuit **31**, liquid crystal cell **32**, and a backlight **33**. The liquid cell control circuit **31** consists of panel drivers such as an LCD controller LSI **34**, a source driver (X driver) **35**, and a gate driver (Y driver) **36**. The LCD controller LSI **34** processes signals received from the I/F board **20** via a video interface and outputs appropriate signals to each ICs of the source driver **35** and gate driver **36** with an appropriate timing. The liquid crystal cell **32** outputs an image using a TFT array arranged in a matrix through the application of a voltage from the source driver **35** and the gate driver **36**. The backlight **33** has a fluorescent tube (not shown) located on the back or side of the LC cell **32** for illuminating the cells from the back.

FIG. **2** is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line **51** indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line **50** indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

Consider the case where a wire-frame model of a halftone, which is 50% brightness, is displayed on the LCD having the characteristics shown in FIG. **2**. In the stationary state **51**, there is no problem because the 50% brightness of a pixel can be achieved with some frames by driving the liquid crystal with a voltage providing the 50% brightness. On the other hand, in the moving state, as apparent from the line **50** indicating the brightness for the R signal in moving state, actually only 21% brightness can be obtained on the display even by driving the liquid crystal with a voltage equivalent to 50% brightness. To achieve an actual brightness of 50%, the LC must be driven with an voltage equivalent to 83% brightness. That is, an offset of 33% is required to be applied to the input voltage equivalent to 50% brightness. For the B signal, more offset is required. Though the brightness for G signal is somewhat closer to that in the stationary state **51**, an offset is still required to be applied.

The relationship between the response characteristic of liquid crystal and flicker will be further discussed below.

FIG. **3** is a table showing the measurements of the response time of liquid crystal at the maximum brightness in five LCD models (models A to E). In a model **61** shown in the first column, the symbol in parentheses indicates the magnitude of flicker at the maximum brightness. Symbol "○" indicates that almost no flicker is visually perceived, symbol "Δ" indicates that flicker level is quite acceptable, and symbol "X" indicates that intensive flicker is perceived. Response rising time **62** is shown in the second column and response falling time **63** is shown in the third column. The light quantity ratio **64** in the forth column represents the ratio of the light quantity of each model to that of an ideal LC. The ratio of the brightness of the drawing in a moving state to that in a stationary state **65** is indicated in the fifth column. The brightness ratio of the drawing in moving state to that in stationary state **65** represents to what degree the brightness of the wire-frame model in the moving state is darkened compared to the brightness of that in the stationary state. It can be seen that while there is almost no reduction in brightness in model A (1.0:1), brightness is reduced in models B (0.8:1), D (0.7:1), and E (0.3:1), on which flicker is perceived.

In terms of whether the response at the maximum brightness is adequately fast, both of the response rising time **62** and the falling time **63** of model A is poor compared to model B. However, when a wire-frame model in an actual CAD application is displayed and moved on these LCD models, flicker in model A is less than in model B. The reason can be explained by considering the characteristics of human visual perception. It is known that the human visual perception is subject to a time integration effect ("Handbook of information technology for television image", 1st edition, pp.39–40, Institute of Television Engineers of Japan, 1990). Brightness of a pixel to the human eye cannot be considered in terms of time required to reach a specified brightness, instead, it should be considered in terms of the quantity of light, that is, a brightness change integrated with respect to time.

FIG. **4** shows the response characteristic of an ideal liquid crystal and indicates the state in which a particular pixel is kept lit up at a brightness of L**1**, that is in a stationary state. Here, the quantity of light (S) emitted in one frame time (T) is equal to L1×T (i.e. brightness×time) as shown in the shaded area in FIG. **4**.

FIGS. **5**A and **5**B show the response characteristic represented by brightness versus time when a pixel stays lit up for one frame time (On→Off) in models A, B shown in FIG. **3**. Both of the rising and falling of the response of model A shown in FIG. **5**A are gradually. As a result, the quantity of light (S_A') which is almost the same as that in the ideal LC shown in FIG. **4** can be obtained ($S_A' \approx S$). On the other hand, even though the response rising of model B is rapid, the falling is also rapid and steep as shown in FIG. **5**B. Accordingly, quantity of light S_B' is only 81% of that of the ideal LC as shown the column "Light quantity ratio" **64** in FIG. **3**. Therefore, even though the response time of model B is better than that shown in FIG. **5**A, there is a difference in brightness (the brightness in model B is less than model A) due to the difference in light quantity ($S_B' < S_A'$) in stationary/moving states, causing flicker when the wire-frame model is moved on model B. As can be seen from the results for models C, D, E in FIG. **3**, displays providing a smaller light quantity ratio **64** provide a smaller brightness ratio **65** of a drawing in a moving state to that in a stationary state, resulting in more flicker.

Although the ultimate solution to these problems is to develop an LC device having an ideal response characteristic as shown in FIG. **4**, it will be some time before such a device comes into use. Thus, another solution is required for inhibiting flicker even in LC devices having moderate response time.

One of the effective solutions may be a method that uses the measurement of a brightness difference between the stationary state **51** and moving state **50** as shown in FIG. **2**. That is, a wire-frame model is drawn with an adequate gray scale by taking account of a required offset, which can be read from the graph shown in FIG. **2**, during the movement of the wire-frame model.

FIG. **6** shows an effect when brightness is set by taking a required offset into account. If the liquid crystal is driven trying to achieve desired brightness L1 as target, only the quantity of light (S') indicated by reference number **71** can be obtained due to the response time of the liquid crystal described above. The quantity of light (S') **71** is much smaller than the quantity of light (S) provided by the ideal response characteristic shown in FIG. **4**. On the other hand, if the liquid crystal is driven with the aim of achieving brightness L2 which is larger than the desired brightness of L1, the quantity of light (S") indicated by reference number **72** can be obtained. By overdriving the LC to brightness L2, the LC reaches L1 in a short response time and the quantity of light (S") **72** can be obtained which is approximately the same as the quantity of light (S), which would be provided with the ideal response characteristic (S"≈S). Here, optimum brightness L2 with respect to L1 can be obtained from the data shown in FIG. **2**.

FIG. **7** is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table **26** stored in the ROM **23** shown in FIG. **1**. The content of the graph base table **26** shown in FIG. **7** represents a relation between the previous brightness and the next brightness for the LC cell **32** having the characteristic shown in FIG. **2**, by taking the effect shown in FIG. **6** into consideration. The previous brightness can be obtained from a video signal input through the ASIC**21** shown in FIG. **1** and stored in the frame buffer **22**. The next brightness can be obtained from the next video signal input to the ASIC **21**. The graph base table **26** is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell **32**.

The first row of the graph base table **26** shown in FIG. **7** indicates brightness output for the next brightness when the previous brightness is 0 and match the readings of the R signal in the moving state line **50** in the graph shown in FIG. **2**. For example, if the next brightness is "10", find a value of 10% on the vertical scale and follow the horizontal line from that point to the point at which the line intersects the moving state line **50**, and a value 28%, which is the desired brightness, can be read. When brightness rises from a certain halftone to another halftone, the offset difference is added to the previous brightness. For example, if the previous brightness is 10 and the next brightness is 20, then (48−28)+10=30. If the next brightness is 30, then (63−28)+10 =45. Similarly, if the previous brightness is 20 and the next brightness is 30, then (63−48)+20=35. If the previous brightness is 30 and the next brightness is 40, then (74−63)+30=41. In this embodiment, if a difference between the previous brightness and the next brightness is greater than an offset, the next brightness is output without change. For example, if the previous brightness is 10 and the next brightness is 80, then the offset is (96−28)=68. If the previous brightness value, 10, is added to this offset, the result would be 78. In this case, the brightness of 80 is output in order to ensure the next brightness.

On the other hand, when brightness falls from a certain halftone to another halftone, the offset is subtracted from the previous brightness. The example in FIG. **7** shows a case where the characteristic of the LC cell **32** when brightness rises (the cell is turned on) is the same as that when the brightness falls (the cell is turned off). In this example, if the previous brightness is 100 and the next brightness is 10, the output value will be 100−98=2. The value "98" is equal to the value when the previous brightness is 0 and the next brightness is 90 in FIG. **7**. Similarly, if the previous brightness is 100 and the next brightness is 20, then 100−96=4. If the previous brightness is 90 and the next brightness is 30, then 100−75=25. The value "75" is equal to the value when the previous brightness is 10 and the next brightness is 70 in FIG. **7**. Similarly, if the previous brightness is 90 and the next brightness is 40, then 100−70=30. The value "70" is equal to the value when the previous brightness is 10 and the next brightness is 60 in FIG. **7**.

While in the table in FIG. **7** the values of previous and next brightness are indicated in increments of 10 for clarity, the table in practice is constructed to store all the combinations which can be read from measurements as shown in FIG. **2**. For example, brightness values in increments of 1 may be stored, and any other degree of precision may be chosen according to a given device. While brightness is expressed in percent figures in FIG. **7**, the expression of addresses and value stored in the table is not limited to percentage, instead, any appropriate quantized values manageable in a given circuit may be used.

FIG. **8** is a graph showing brightness desired to be provided versus brightness provided actually when brightness falls. The liquid crystal in the example in FIG. **8** has brightness which falls with exhibiting a characteristic similar to the rising characteristic shown in FIG. **2**. Accordingly, the line **80** indicating a moving state shown in FIG. **8** is the vertically-flipped curve of the line **50** in a moving state shown in FIG. **2**. Tick mark labels on the horizontal scale are also inverted. As can be seen from the graph, when the brightness actually provided is 50%, the brightness desired to be provided is 17%. This matches the value when the previous brightness is 100 and the next brightness is 50 in the table in FIG. **7**. That is, the moving state line **80** in FIG. **8** exactly indicates the fall of the previous brightness from 100% in FIG. **7**.

While the embodiment has been described with respect to the example which exhibits the same rising (from OFF to ON) and falling (from ON to Off) characteristics, these characteristics may vary depending on the types of liquid crystals. Therefore, the embodiment is configured to accommodate the variation of characteristics by modifying the values in FIG. **7** according to the characteristics of a given liquid crystal.

As described above, the embodiment is configured to store offsets in table form based on the relation between a brightness level in a stationary state and that in a moving state in order to obtain an ideal quantity of light. Thus, even during the movement of a display image on the LCD screen, the image can be displayed virtually the same brightness to the eye as in its stationary state, thereby inhibiting flicker on the screen.

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer **22** and a supplementary correction is made by the ASIC **21** using the data in the graph base table **26** based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a wire-frame model is moving or stationary is not required to be determined. Instead, the movement of the model can be determined from a difference between the determined brightness and the previous brightness. As a result, flicker can be inhibited by a simple circuit configuration.

Furthermore, the embodiment addresses the flicker problem resulting from the response time of the LC panel in recognition of the importance of the quantity of light (brightness×time) to visual perception. As a result, slow response of any types of liquid crystals (such as TN, IPS, and MVA) can be compensated by constructing a look-up table adapted to the characteristics of each liquid crystal. Thus, a flexible liquid crystal control circuit and liquid crystal display which can be widely used can be provided.

As described above, according to the invention, flicker of LCDs which poses a considerable problem in applications such as the display of wire-frame model can be made unperceivable to the user's eye by a simple configuration.

While this invention has been described in terms of certain embodiment thereof, it is not intended that it be limited to the above description, but rather only to the extent set forth in the following claims. The embodiments of the invention in which an exclusive property or privilege is claimed are defined in the appended claims.

We claim:

1. A liquid crystal display, comprising:

an input logic for inputting a video signal from a host;

a storage for storing the previous brightness level of the video signal input through said input logic;

a determinator for determining an output brightness level based on the previous brightness level stored in said storage and the next brightness level of the next video signal input to said input logic so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level; and

a driver for driving an image displaying liquid crystal cell based on said output brightness level determined by said determination logic.

2. The liquid crystal display according to claim **1**, wherein said determinator comprising a table for storing a brightness level determined by the characteristic of a liquid crystal cell according to a relation between the previous brightness level and the next brightness level, and determining the output brightness level by modifying said next brightness level based on the brightness level read from said table.

3. The liquid crystal display according to claim **2**, wherein:

said video signal input through said input logic comprises a plurality of color signals; and

said table in said determinator is provided for each of said color signals.

4. A liquid crystal display, comprising:

a driver for driving each of the pixels forming an image for each frame to a liquid crystal cell displaying said image;

an input logic for inputting a moving-state video signal which changes from the on state to the off state on transition to a particular frame in said frames and returns to the off state after said particular frame is completed;

a setting logic for setting an offset for making the quantity of light closer to the quantity of light in a stationary state in which said moving-state video signal is continuously turned on for said particular frame;

a generator for applying said offset set by said setting logic to said moving-state video signal input through said input logic to generate an output video signal; and

an output logic for outputting said output video signal generated by said generator to said driver.

5. The liquid crystal display according to claim **4**, wherein said offset set by said setting logic can be determined based on a time integration quantity and the quantity of light in said stationary state, said time integration quantity being a change in brightness in said moving-state vide signal integrated with respect to time.

6. The liquid crystal display according to claim **4**, wherein:

said moving-state video signal input through said input logic comprises a plurality of color signals;

said offset set by said setting logic is determined for each of said color signals; and

said generator generates the output video signal for each color signal based on said offset determined for each color signal.

7. A liquid crystal control circuit, having a function for inhibiting flicker caused by a difference in brightness when an input wire-frame model is displayed by liquid crystal cells, comprising:

a storage portion for storing an offset in brightness in a moving state in which said wire-frame model having a predetermined gray scale changes from frame to frame with respect to a particular pixel, with relation to brightness output in a stationary state in which the wire-frame model having the predetermined gray scale is displayed on the particular pixel across a plurality of frames; and

a correction portion for applying said offset stored in said storage portion to the gray scale of the wire-frame model if said input wire-frame model is in a moving state.

8. The liquid crystal control circuit according to claim **7**, further comprising a frame buffer for storing the brightness information of said input wire-frame model as the previous brightness,

wherein said storage portion stores said offset as table information based on a relation between said previous brightness stored in said frame buffer and the brightness of the next input wire-frame model.

9. A flicker inhibition method for inhibiting flicker caused by a difference in brightness when an input wire-frame model is displayed by a liquid crystal cell, comprising the steps of:

storing a relation between brightness in a stationary state in which a wire-frame model having a predetermined gray scale is displayed on a particular pixel and a plurality of frames and brightness in a moving state in which the wire-frame model having the predetermined gray scale changes frame to frame with respect to the particular pixel;

applying an offset based on said stored relation to the gray scale of said wire-frame model if said input wire-frame model is in a moving state; and

driving said liquid crystal cell based on said gray scale to which said offset is applied to display said wire-frame model.

10. The flicker inhibition method according to claim **9**, wherein said storing step said moving state brightness used for storing said relation is the brightness when said particular pixel changes back to the off state one frame after said particular pixel is driven from the off state to the on state during the passage of the wire-model frame over the particular pixel.

11. The flicker inhibition method according to claim **9**, wherein said storing step said brightness in the moving state which is used when said relation is stored is the quantity of light equal to a brightness change integrated with respect to time.

12. A liquid crystal driving method, comprising the steps of:

storing first brightness information for an input pixel in a frame buffer;

applying based on second brightness information for the next input pixel and said first brightness information stored in said frame buffer an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state to said second brightness information;

outputting said second brightness information to which said offset is applied to a driving circuit for driving an liquid crystal cell; and

storing said second brightness information for the input pixel in a frame buffer.

13. The liquid crystal driving method according to claim 12, wherein:

said step of storing said first brightness information in the frame buffer stores said first brightness information for each of said color signals and said input pixel comprises a plurality of color signals; and

said step of applying the offset applies said offset to each of said color signals.

14. The liquid crystal driving method according to claim 12, wherein said offset applying step comprises the steps of reading a pre-stored offset based on a relation between said first and second brightness information and applying said read offset to said second brightness information.

* * * * *

EXHIBIT F

US006689629B2

(12) **United States Patent**
Tsujimura et al.

(10) **Patent No.: US 6,689,629 B2**
(45) **Date of Patent: Feb. 10, 2004**

(54) **ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 54 days.

(21) Appl. No.: **10/068,500**

(22) Filed: **Feb. 5, 2002**

(65) **Prior Publication Data**

US 2002/0106843 A1 Aug. 8, 2002

(30) **Foreign Application Priority Data**

Feb. 6, 2001 (JP) 2001-029587

(51) **Int. Cl.**[7] **H01L 21/00**

(52) **U.S. Cl.** **438/25**; 438/149; 438/73; 257/72; 257/748

(58) **Field of Search** 438/25, 22, 30, 438/149, 73; 257/72, 748

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(57) **ABSTRACT**

Disclosed is to provide an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.

The present invention is an array substrate for display, which includes: a thin film transistor array formed on an insulating substrate **1**; a plurality of wirings **23** and **24** arranged on the insulating substrate **1**; connection pads **25** and **27** arranged on unilateral ends of the wirings **23** and **24** and respectively connected therewith; and pixel electrodes **22**, wherein dummy conductive patterns **29** are arranged between the ends of the connection pads **25** and **27** and ends of the pixel electrodes **22**.

16 Claims, 11 Drawing Sheets

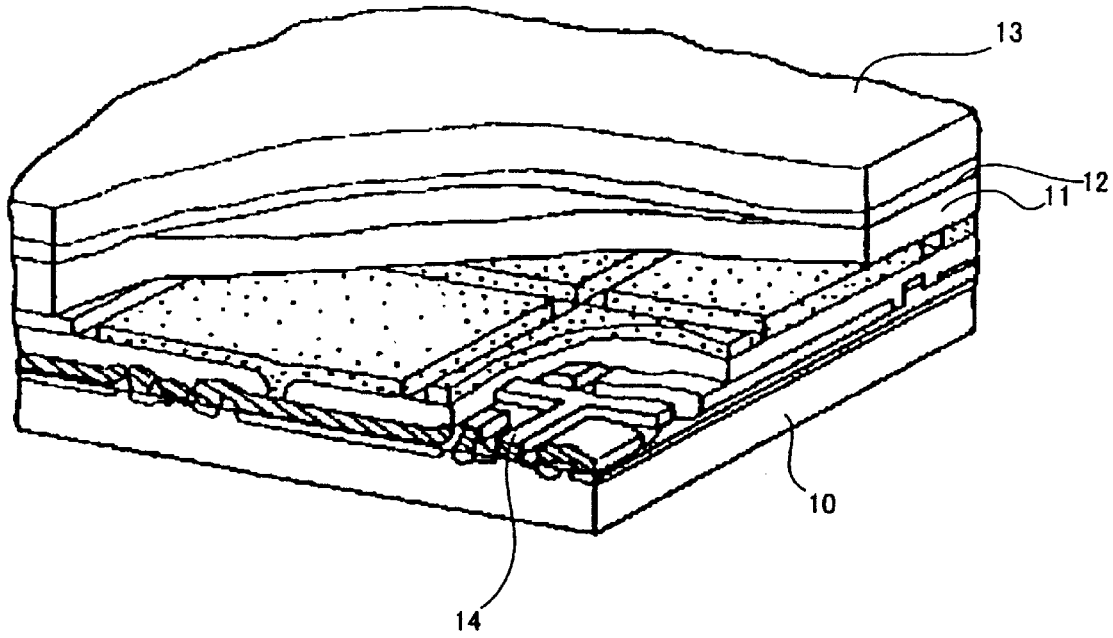


FIG. 1

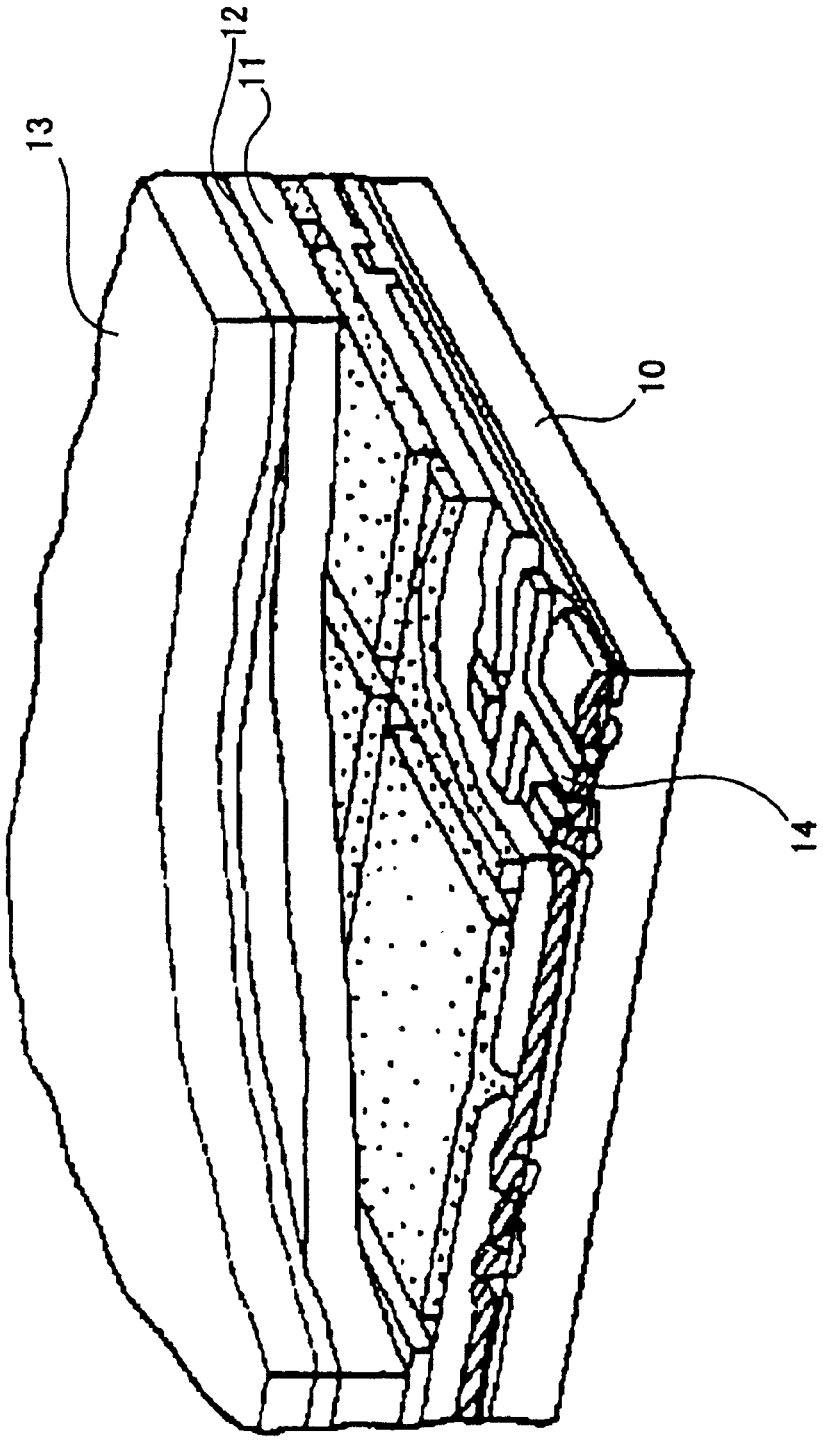


FIG. 2

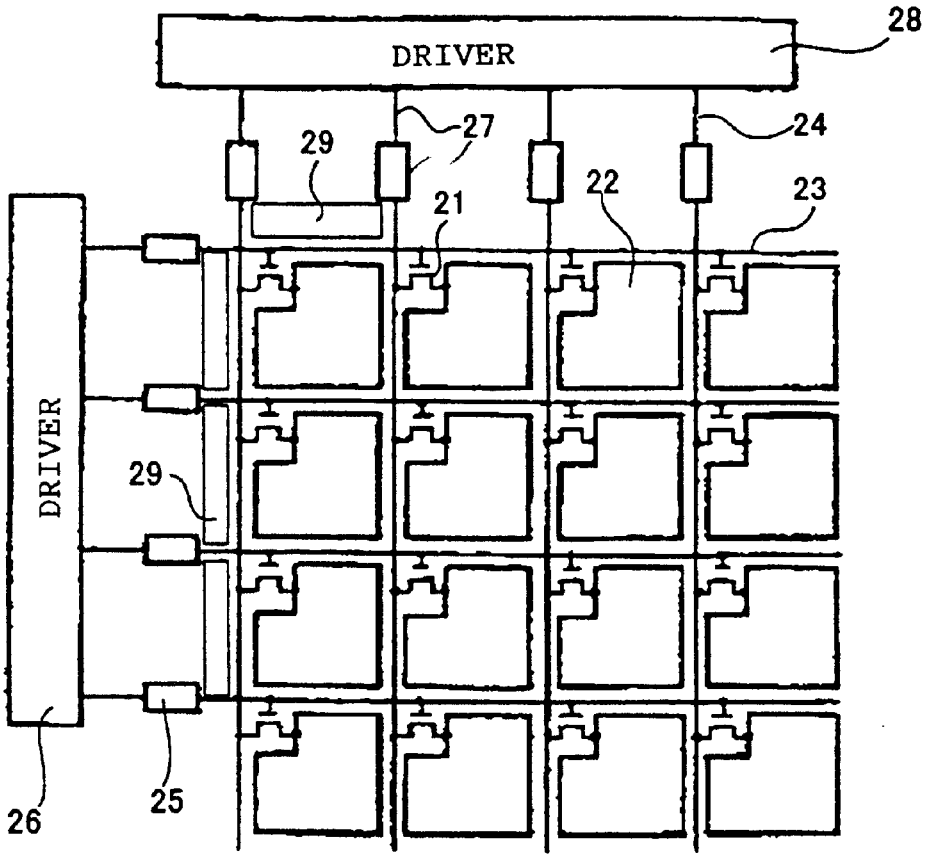


FIG. 3

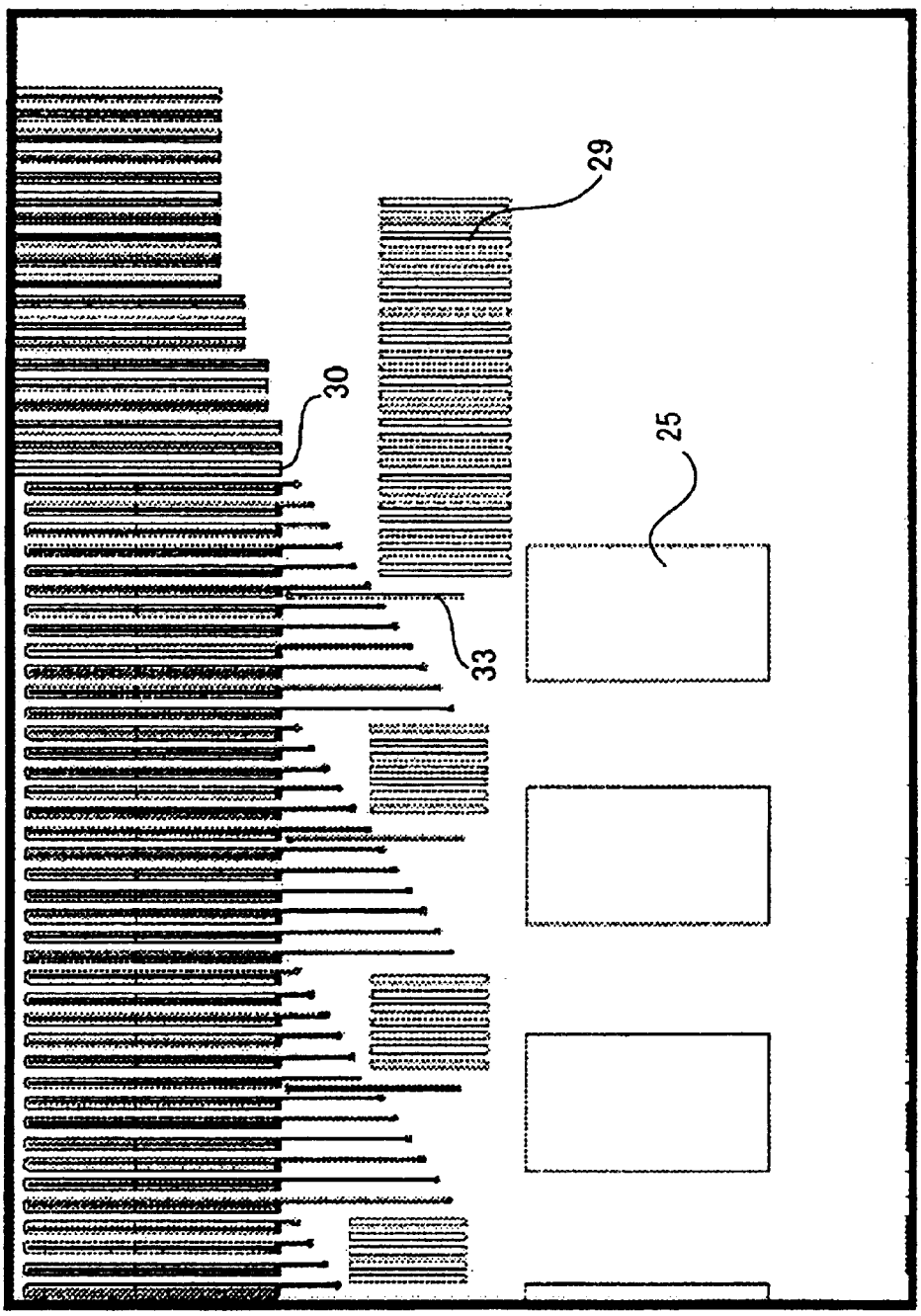


FIG. 4

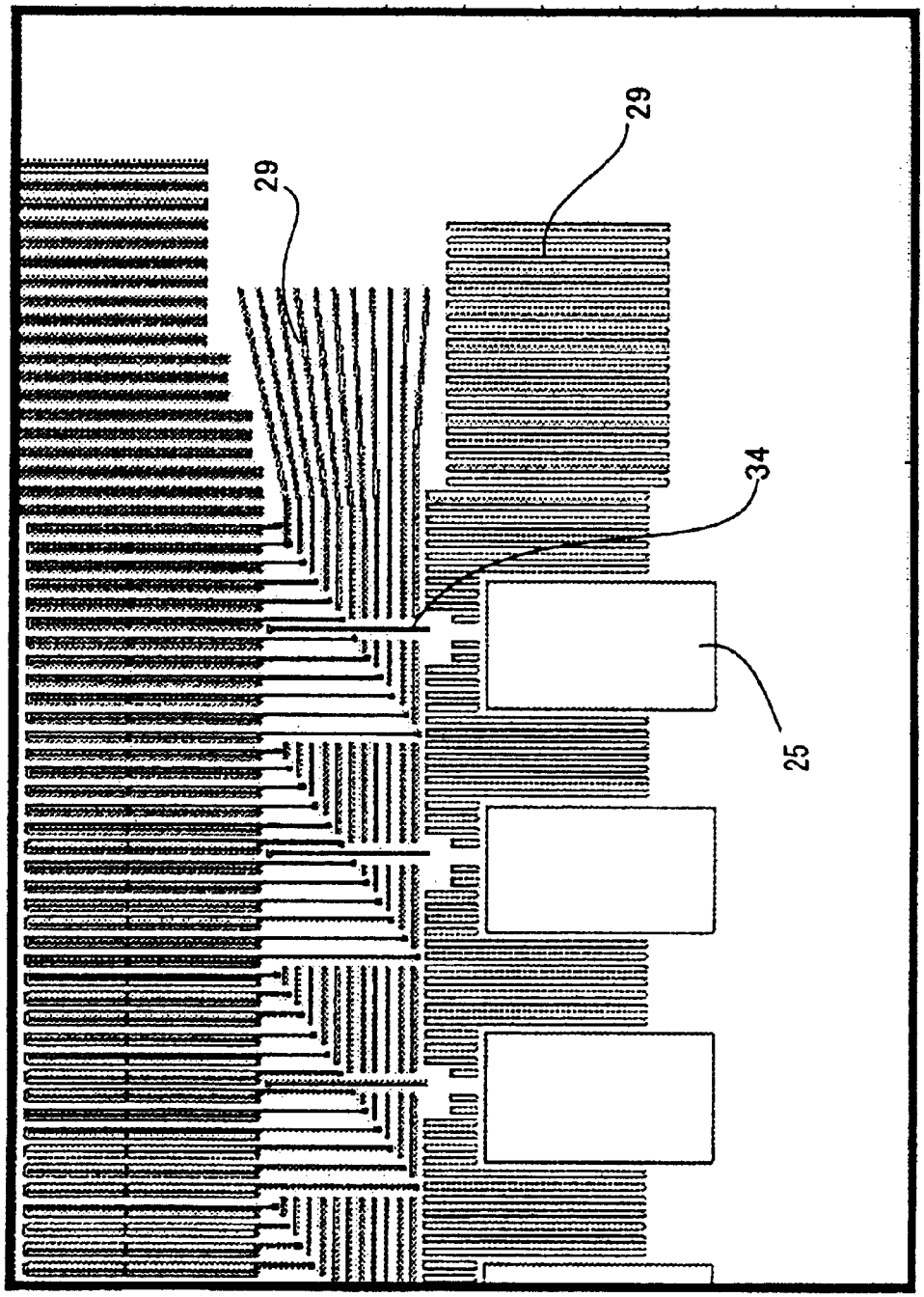


FIG. 5

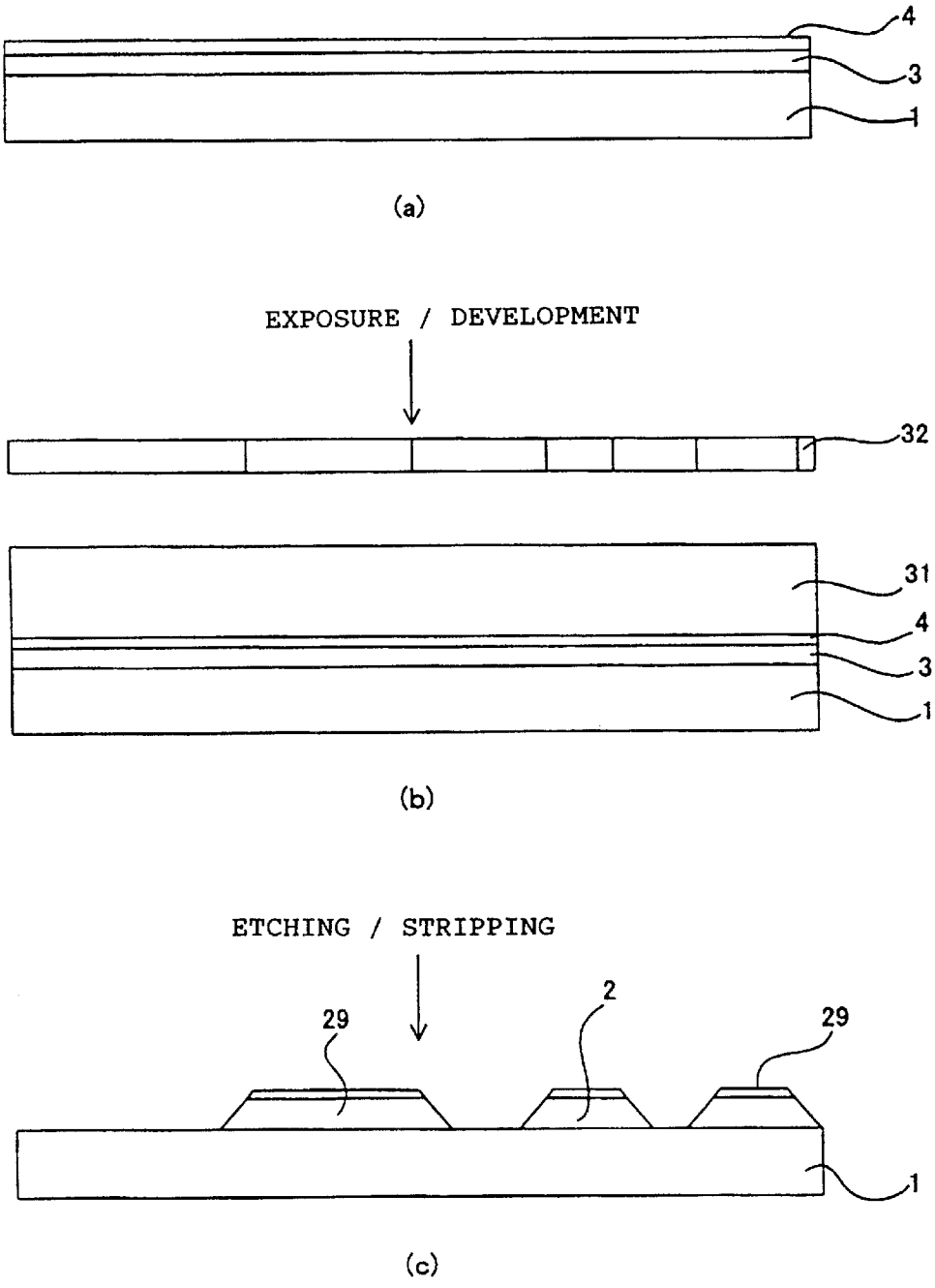

4
3
1
(a)
EXPOSURE / DEVELOPMENT
32
31
4
3
1
(b)
ETCHING / STRIPPING
29
2
29
1
(c)

FIG. 6

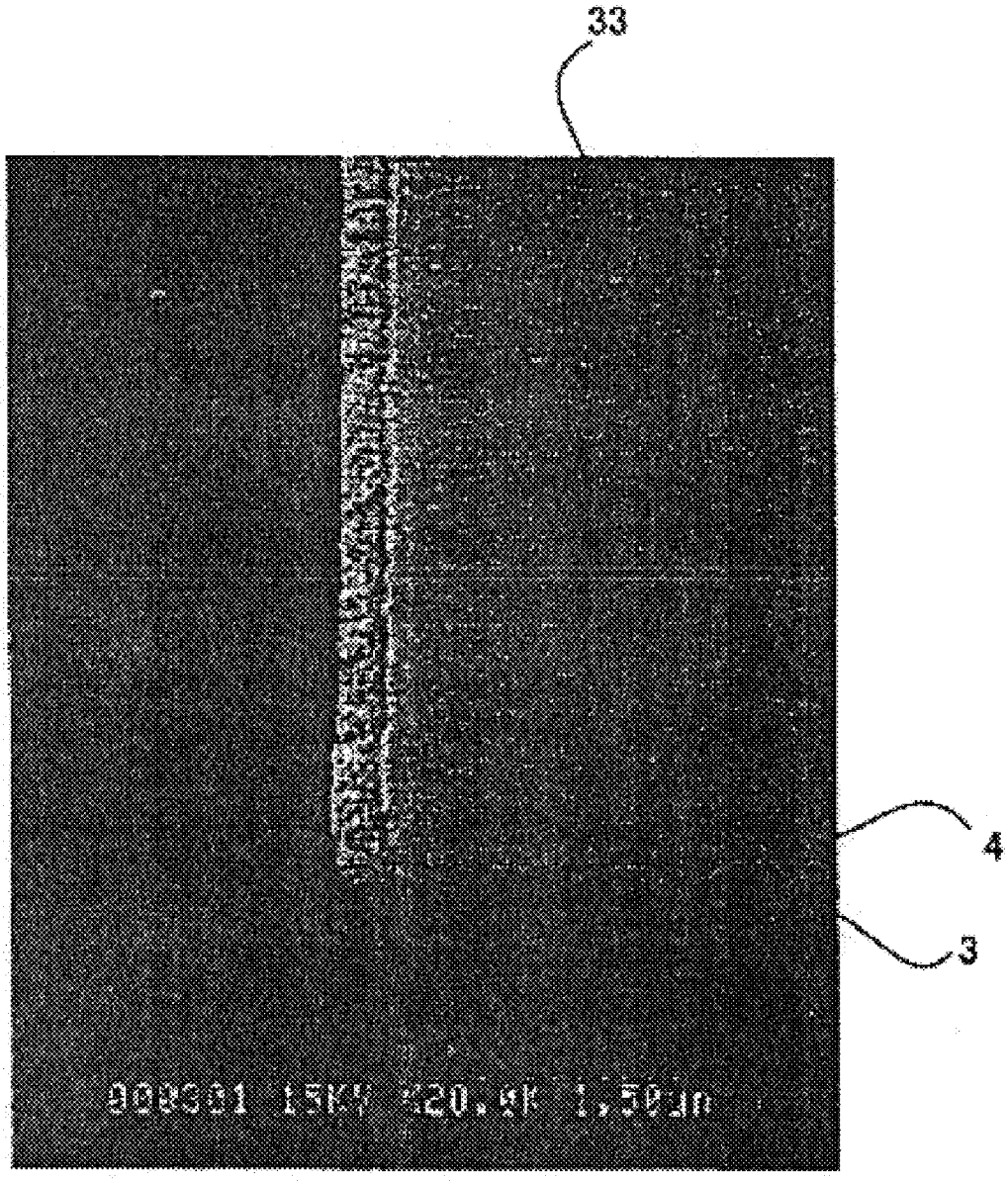


FIG. 7

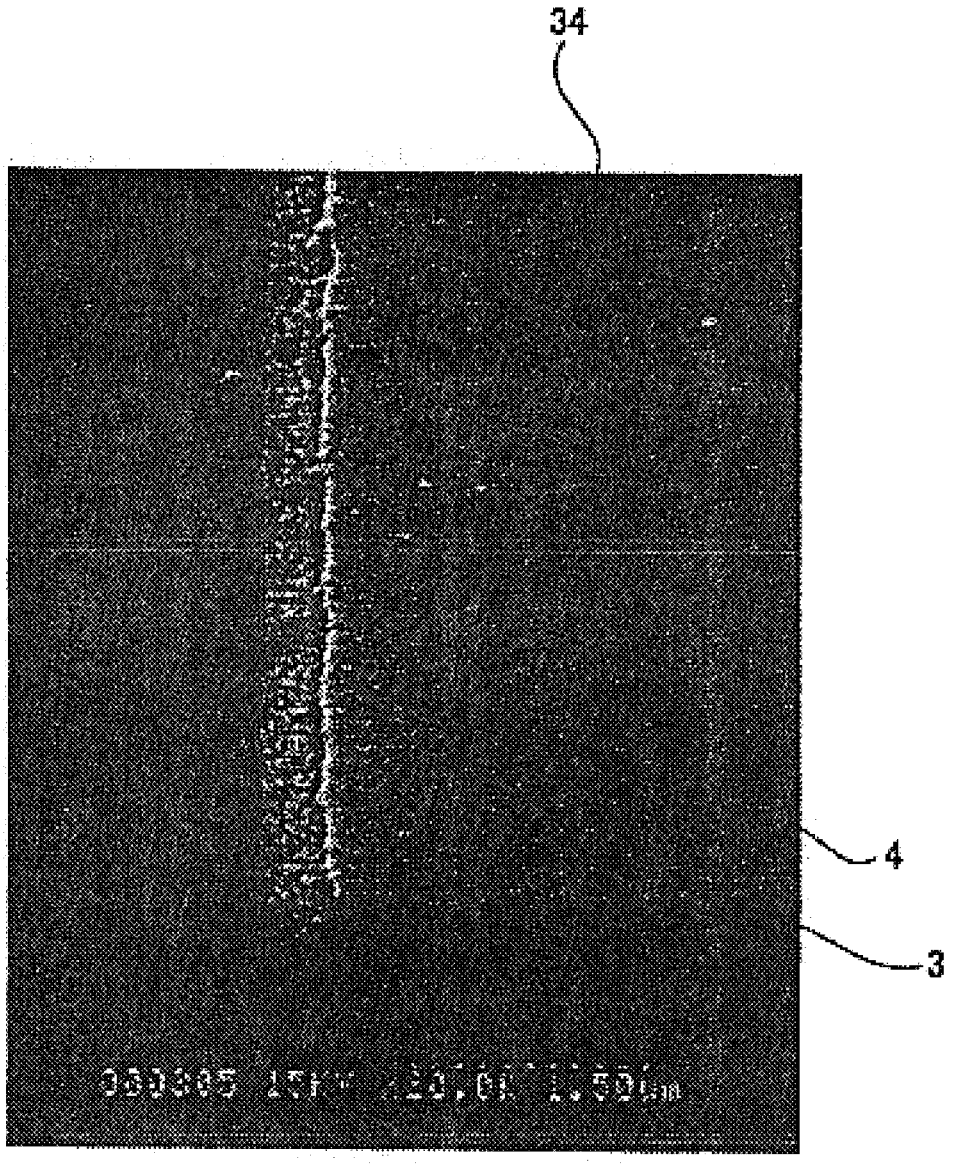


FIG. 8

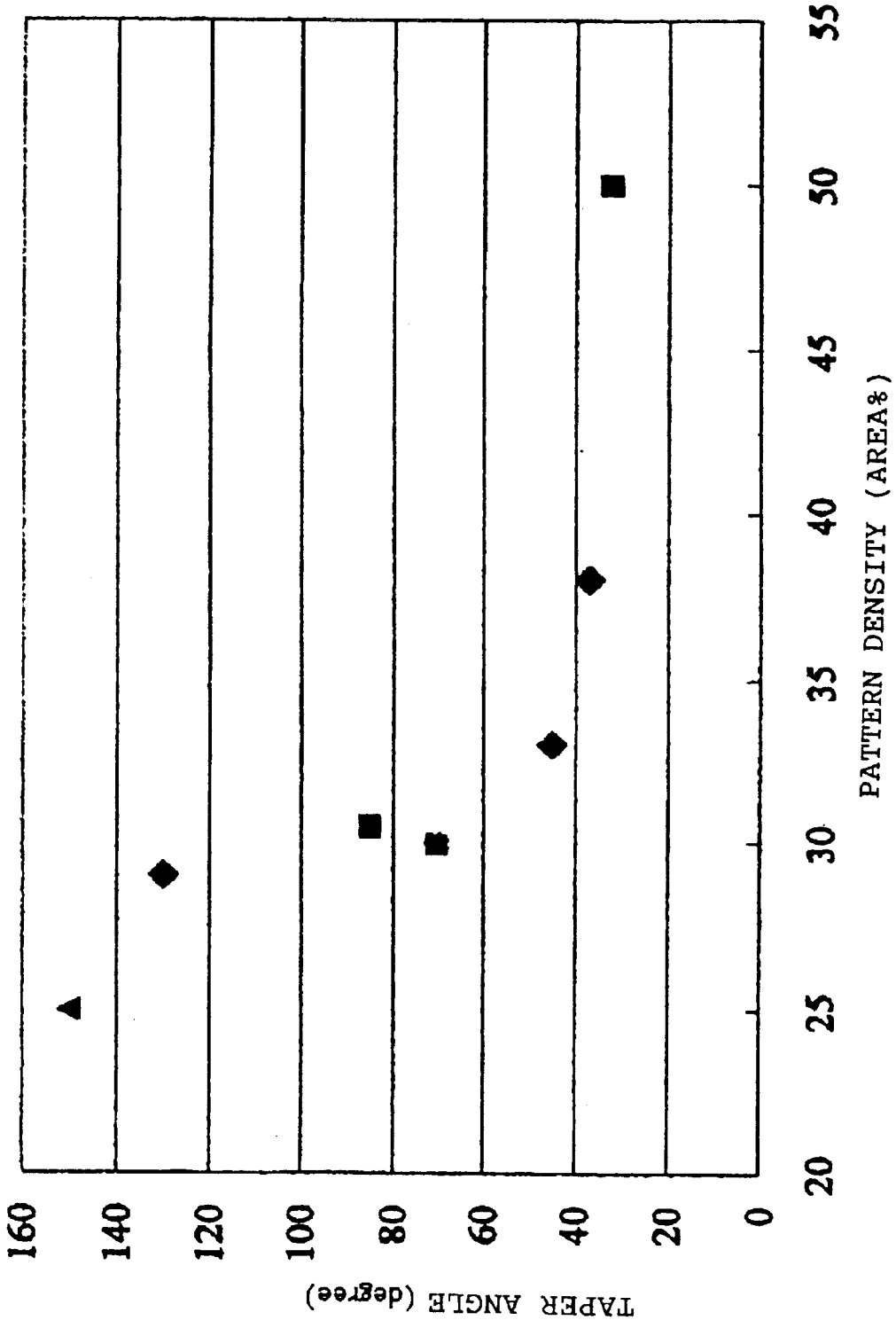

TAPER ANGLE (degree)
160
140
120
100
80
60
40
20
0
PATTERN DENSITY (AREA%)
20
25
30
35
40
45
50
55

FIG. 9

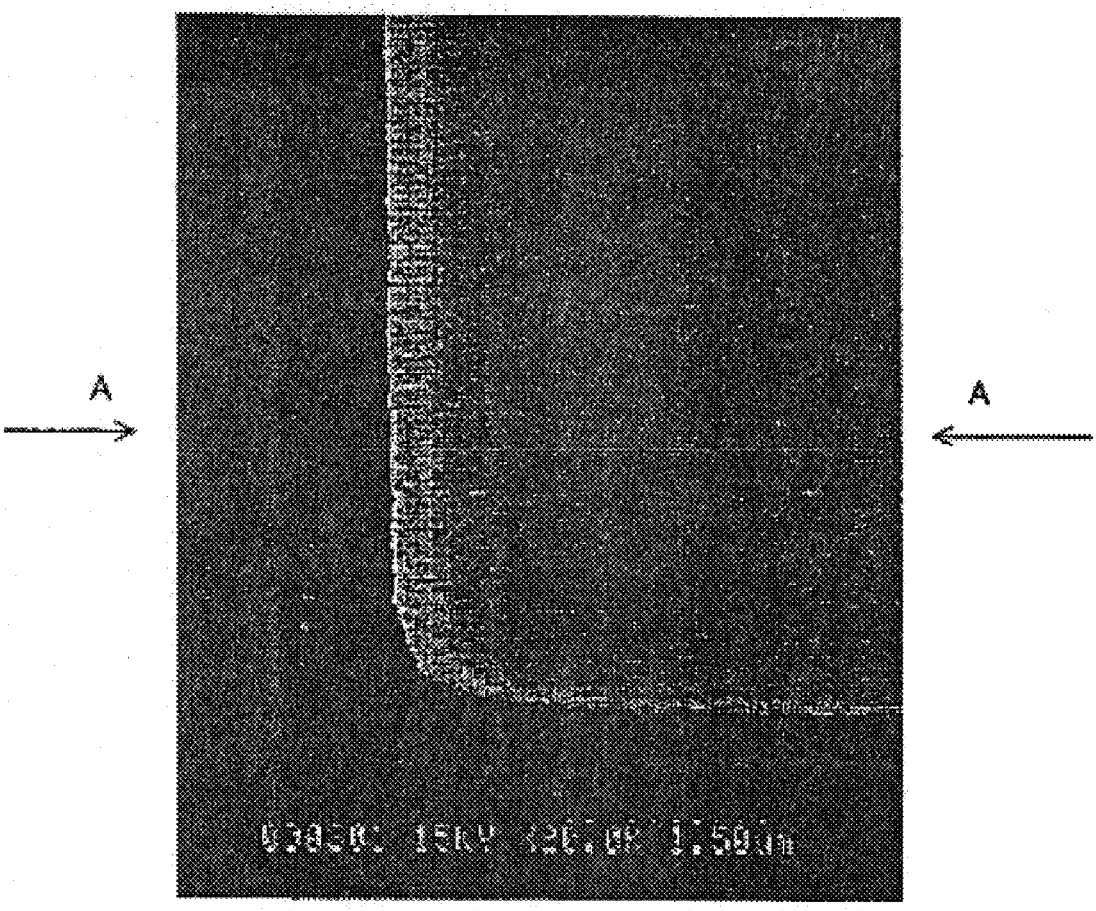


FIG. 10

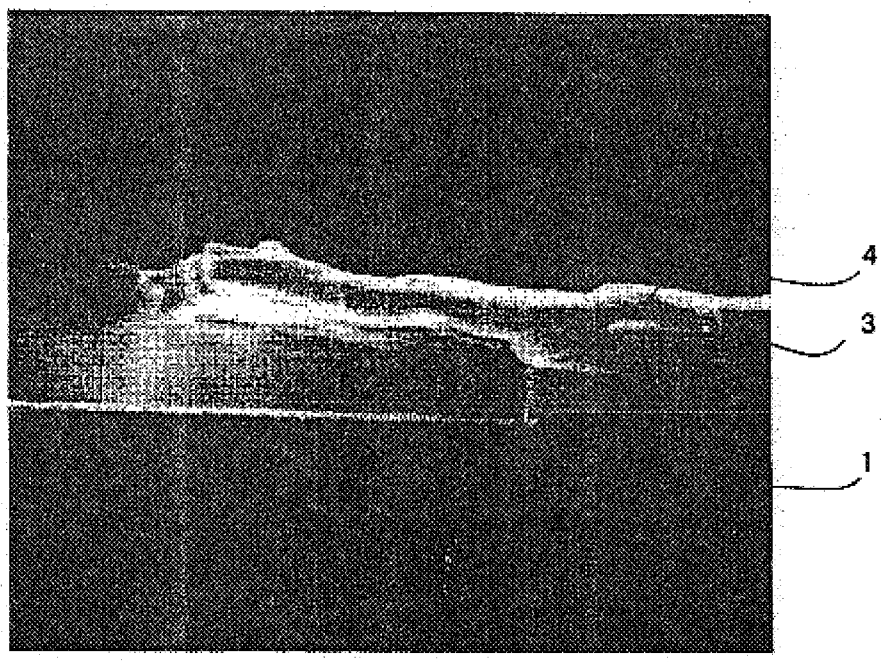


FIG. 11

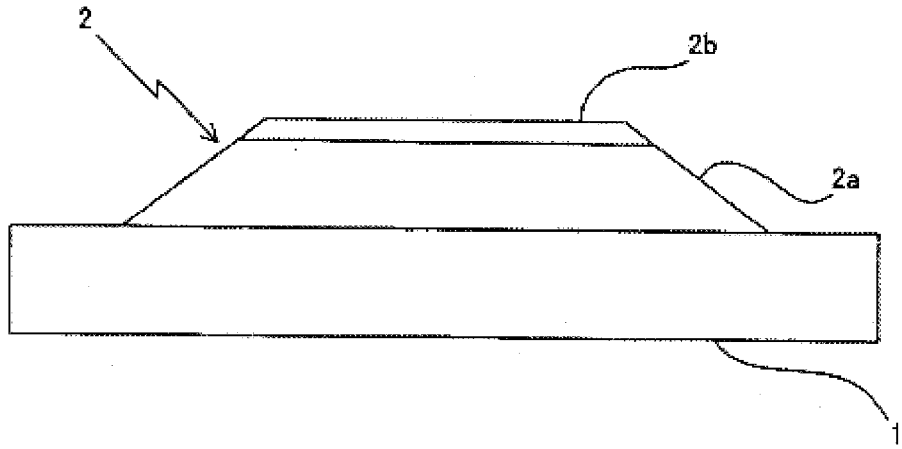
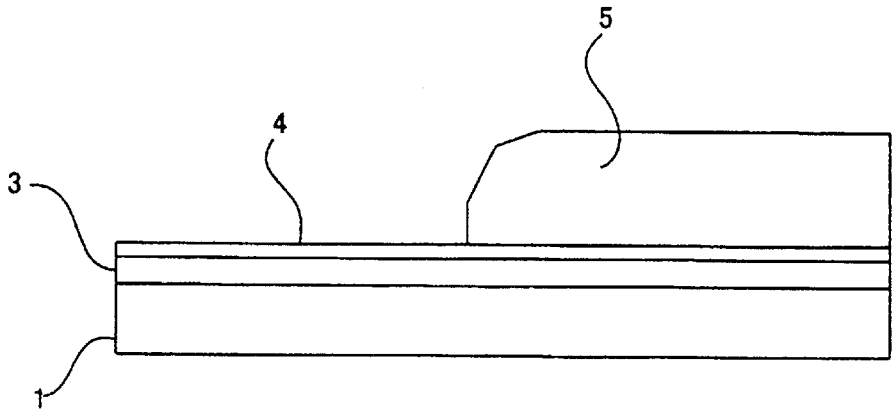
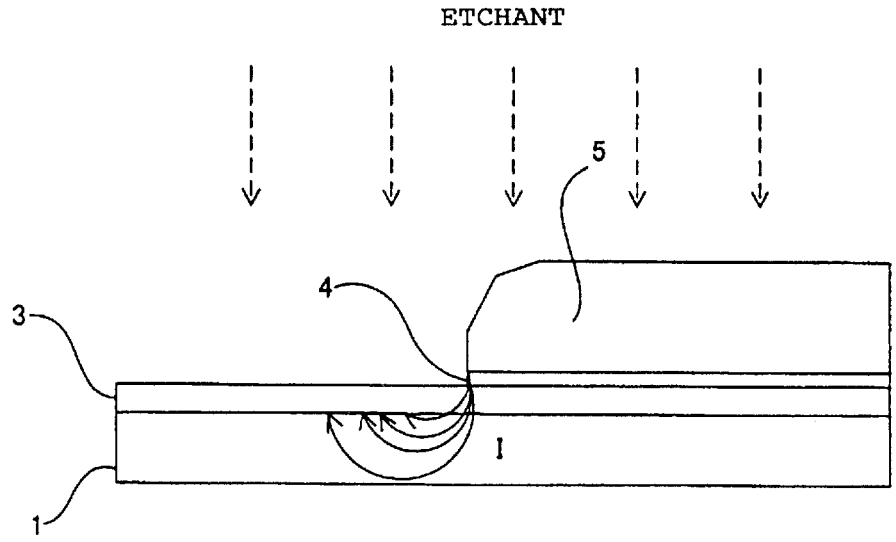


FIG. 12



(a)



(b)

ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

BACKGROUND OF THE INVENTION

The present invention relates to an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.

A display device using a thin film transistor (TFT) array has been frequently used owing to low power consumption and capability of downsizing the display device. The thin film transistor array is manufactured by forming thin film transistors, each being composed of electrodes such as a gate electrode, a source electrode and a drain electrode, wirings such as scan lines and signal lines connected with the above-mentioned electrodes, and pixel electrodes on an insulating substrate.

In recent years, a higher operating speed, a higher resolution and a larger size have been required for the display device described above in many cases. A high speed and a high density have been required for each constituent component of the array for display, which forms a display device. Particularly, in order to operate the thin film transistor array at a high speed, it is preferable to use low-resistance aluminum (Al) for the wirings such as the scan lines and the signal lines since delay in gate pulses can be reduced and a writing speed to the thin film transistor can be increased.

Incidentally, aluminum tends to be easily oxidized in spite of its low resistance. Therefore, in many cases, wiring using aluminum is constituted as a two-layer structure, in which aluminum is used as a lower conductive material, and a material harder to be oxidized than aluminum such as chromium, tantalum, titanium or molybdenum is used as an upper conductive material. FIG. **11** is a view schematically showing a state where wiring **2** is deposited on an insulating substrate **1**. A lower conductive material film **2***a* is deposited on an insulating substrate **1** made of such as glass, and an upper conductive material film **2***b* is deposited on the lower conductive material film **2***a*. Each of these films **2***a* and **2***b* is patterned by, for example, a proper etching process so as to have tapered ends.

In order to form a tapered shape shown in FIG. **11**, an etching rate for the upper conductive material is required to be increased. In order to form the tapered shape shown in FIG. **11**, various methods have been proposed up to now. For example, in the gazette of Japanese Patent Laid-Open No. Hei 10 (1998)-90706, a method has been proposed, in which dummy connection pads are provided on sides opposite to scan line connection pads and signal line connection pads, respectively. According to this method, over etching due to an etchant that will be relatively increased by lowering wiring density at ends of the substrate is prevented. Thus, undercut of a lower conductive material **3** is prevented, and an interlayer short circuit is prevented by imparting a proper tapered shape to the wiring **2**.

However, though this method enables evenness of etching at the ends of the thin film transistor array substrate to be improved, the method cannot effectively prevent the undercut of the signal lines in a region where the wiring density is apt to be lowered from ends of the pixel electrodes to the connection pads, for example, in a portion where drawing wiring is formed.

Moreover, in the gazette of Japanese Patent Laid-Open No. Hei 10 (1998)-240150, disclosed is a method of forming a tapered shape at an angle ranging from 20 degrees to 70 degrees on wiring constituted of two layers, in which a pad formed of aluminum and metal such as molybdenum formed on the aluminum is subjected to wet etching. According to this method, a specified tapered shape can be imparted to the wiring formed of a conductive film of a two-layer structure by the wet etching. However, the method never discloses a method of evenly etching a substrate region while maintaining a selection ratio thereof even in the substrate region where the wiring density is lowered.

FIGS. **12**A and **12**B are enlarged schematic views for explaining a patterning process using a conventionally used wet process in order to impart the above-described tapered shape to the wiring. As shown in FIG. **12**A, the lower conductive material **3** and an upper conductive material **4** are deposited on the insulating substrate **1** by a method such as physical vapor deposition. FIG. **12**A shows that a photoresist film **5** is coated on a film of the upper conductive material **4** and is patterned in a desired shape. The respective films are etched by an etchant such as a solution of phosphoric acid, nitric acid, acetic acid or mixtures thereof, and desired tapered shapes are formed thereon.

FIG. **12**B is a view for explaining an electrochemical process generated as each film is being etched when the wiring constituted of the upper conductive material **4** and the lower conductive material **3** is subjected to wet etching. In FIG. **12**B, an internal layer portion of the upper conductive material **4** coated with the photoresist film **5** is not dissolved. However, at the end of the photoresist film **5**, the upper conductive material **4** is dissolved by the etchant. When the wiring is formed by the wet etching, the upper conductive material **4** protected by the photoresist film **5** is further dissolved in a lateral direction from the end of the photoresist film **5** to turn into positive ions, and electrons emitted as a result are supplied to the lower conductive material **3**. Thus, the upper conductive material **4** serves as an anode. In this connection, the lower conductive material **3** comes to serve as a cathode. Accordingly, an electrochemical cell is formed. Here, when the etching rate for the upper conductive material **4** is increased to form a required tapered shape, the density of the electrons generated by dissolving the upper conductive material **4** and flowing to the lower conductive material **3** is increased accompanied with an increase of a dissolution rate of the upper conductive material **4**. FIG. **12**B schematically shows currents I flowing from the upper conductive material **4** to the lower conductive material **3**.

As the etching rate is increased, the density of the current flowing to an area of the upper conductive material **4**, which is exposed to the etchant, exceeds a current density causing passivity of the upper conductive material **4**. In such a case, the upper conductive material **4** is passivated not to be dissolved by the etchant, and only the lower conductive material **3** is dissolved accompanied with the progress of the etching, resulting in the occurrence of the undercut. When such undercut occurs, the wiring, for example, the gate wiring cannot be sufficiently coated with an insulating film in some cases, thus causing inconvenience such as an interlayer short circuit, resulting in lowering a yield of the display device.

SUMMARY OF THE INVENTION

The present invention was made with the foregoing problems in mind. An object of the present invention is to

provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of being etched at a sufficiently high etching rate and a sufficient selection ratio, eliminating undercut, and providing a large-sized and high-resolution display device.

The foregoing object of the present invention is achieved by providing the array substrate for display, the method of manufacturing an array substrate for display and the display device using the array substrate for display of the present invention.

Specifically, according to the present invention, provided is an array substrate for display, comprising: a thin film transistor array formed on an insulating substrate; a plurality of wirings arranged on the insulating substrate; connection pads arranged on unilateral ends of the wirings and respectively connected with the wirings; pixel electrodes, and dummy conductive patterns arranged between the ends of the connection pads and ends of the pixel electrodes. The dummy conductive patterns can occupy 30 area % or more. In the present invention, the dummy conductive patterns can be formed as any of land patterns and line-and-space patterns. In the present invention, the wirings are constituted of a lower conductive material and an upper conductive material, and the lower conductive material can be any one of aluminum and an aluminum alloy. In the present invention, the upper conductive material has a passivating potential. The upper conductive material can be any one of molybdenum and a molybdenum alloy.

According to the present invention, provided is a method of manufacturing an array substrate for display, the method comprising the steps of: forming a thin film transistor array including: a plurality of wirings arranged on an insulating substrate; and connection pads arranged on unilateral ends of the wirings and respectively connected with the wirings; forming pixel electrodes; and forming dummy conductive patterns between ends of the connection pads and ends of the pixel electrodes. In the present invention, it is preferable that the dummy conductive patterns be formed so as to occupy 30 area % or more. In the present invention, the dummy conductive patterns can be formed as any of land patterns and line-and-space patterns. In the present invention, the wirings are constituted of a lower conductive material and an upper conductive material, the lower conductive material can be any one of aluminum and an aluminum alloy, and the upper conductive material can be any one of molybdenum and a molybdenum alloy. In the present invention, the wirings are formed by wet etching.

Moreover, in the present invention, provided is a display device, comprising the array substrate for display mentioned above.

In the present invention, the display device used as a liquid crystal display device or an electroluminescence display device can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings.

FIG. **1** is a view showing an embodiment of a liquid crystal display device using an array substrate for display of the present invention.

FIG. **2** is a top plan view of the array substrate for display of the present invention.

FIG. **3** is an enlarged view showing a dummy conductive pattern in the present invention.

FIG. **4** is an enlarged view showing another dummy conductive pattern in the present invention.

FIGS. **5**A to **5**C are views illustrating a method of manufacturing the array substrate for display of the present invention.

FIG. **6** is an electron microscope photograph showing a pattern shape of wiring in the case of using the dummy conductive pattern shown in FIG. **3**.

FIG. **7** is an electron microscope photograph showing a pattern shape of wiring in the case of using the dummy conductive pattern shown in FIG. **4**.

FIG. **8** is a graph showing a relation between a taper angle of the wiring and a pattern density of the wiring.

FIG. **9** is an electron microscope photograph showing a wiring shape in the case of performing etching without using the dummy conductive pattern.

FIG. **10** is an electron microscope photograph showing a sectional shape of the wiring shape shown in FIG. **9**.

FIG. **11** is a schematic view showing a tapered shape of the wiring.

FIGS. **12**A and **12**B are views showing currents formed by a cell formed during an etching process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinbelow, description will be made in detail for the present invention with reference to embodiments shown in the accompanying drawings. However, the present invention is not limited to the embodiments shown in the drawings.

FIG. **1** is a partially cutaway perspective view showing an embodiment of a display device using an array substrate for display of the present invention. As shown in FIG. **1**, the display device of the present invention is constituted by sequentially laminating a liquid crystal layer **11**, a transparent electrode **12** and a glass substrate **13** on an array substrate **10** for display, which is formed on an insulating substrate. Wiring **14** formed on the insulating substrate **10** is extended to an end (not shown) of the array substrate for display, and is connected with a driving system (not shown) through a connection pad (not shown).

FIG. **2** is a top plan view of the display device using the array substrate **10** for display of the present invention, which is shown in FIG. **1**. In the array substrate **10** for display of the present invention, a plurality of thin film transistors **21** constitute an array. A pixel electrode **22** is connected with each thin film transistor **21** that controls a potential of the pixel electrode. In the array substrate **10** for display shown in FIG. **2**, what is further shown is that a scan line **23** and a signal line **24** are connected with each thin film transistor **21**.

The respective scan lines **23** are connected with a driver **26** through scan line connection pads **25**, and the respective signal lines **24** are connected with a driver **28** through signal line connection pads **27**. These scan lines **23** and the signal lines **24** are formed so as to have the same constitution. As shown in FIG. **11**, each of these lines is constituted of the lower conductive material **3** and the upper conductive material **4**.

In the present invention, aluminum can be used for the lower conductive material **3** usable as wiring from a viewpoint of lowering resistance thereof. Moreover, it is preferable to use molybdenum (Mo) for the upper conductive material **4** usable in the present invention from a viewpoint of protecting the aluminum. However in the present invention, besides the aluminum, an aluminum alloy can be used for the lower conductive material **3**. Moreover, for the

upper conductive material **4**, alloys of chromium, tantalum, titanium and molybdenum can be used. Film thickness of the lower conductive material **3** is not particularly limited, but film thickness of the upper conductive material **4** is preferably thick since a current tends to be concentrated thereto as the film thickness becomes thinner. However, a problem regarding stress occurs as the thickness becomes thicker. Therefore, in the present invention, it is preferable to set the film thickness of the upper conductive material **4** in a range of 30 to 100 nm.

The present invention makes it possible to prevent undercut of the lower conductive material **3**, which occurs due to passivity of the upper conductive material **4**. In the present invention, the term "passivity" is referred to as a phenomenon that metal such as molybdenum or a metal alloy such as a molybdenum alloy becomes insoluble in an acid or alkaline etchant. For example, the term "passivity" is referred to as a phenomenon that metal serving as an anode becomes insoluble in such etchant. In the present invention, specifically as for such passivated metal or a metal alloy, metal or a metal alloy with a passivating potential, that is, a Flade potential can be mentioned. Note that, in the present invention, the Flade potential is referred to as a potential which causes a current density for passivating metal, which is described in the Encyclopedia Chimica (miniature edition 32nd printing, issued by Kyoritsu Shuppan Co., Ltd., edited by editorial committee of the Encyclopedia Chimica), vol. 7, p. 911.

Furthermore, in the embodiment shown in FIG. **2**, dummy conductive patterns **29** are disposed between the pixel electrodes **22** and each scan line connection pad **25** and between the pixel electrodes **22** and each signal line connection pad **27**. Thus, the wiring density is increased. Therefore, it is made possible to form good wiring over the entire surface of the array substrate for display without causing defects such as undercut and a mouse hole of the lower conductive material **3** during etching for the scan lines **23** and the signal lines **24**. Each of these dummy conductive patterns **29** can be formed as a two-layers structure with the same materials as those of the scan lines **23** and the signal lines **24** at the same time when the patterning is performed therefor.

FIG. **3** is an enlarged view showing a portion where the dummy conductive pattern **29** is formed in the embodiment of the array substrate **10** for display of the present invention shown in FIG. **2**. FIG. **3** shows the dummy conductive pattern **29** formed as a line-and-space pattern between the connection pad **25** and an end **30** of the pixel electrode. In the present invention, the dummy conductive pattern **29** can be formed as the line-and-space pattern shown in FIG. **3**. Alternatively, the dummy conductive pattern **29** can be formed as a land pattern completely coating a region where the dummy conductive pattern **29** is formed.

In any case of the patterns, in the present invention, it is preferable that the wiring density of the dummy conductive patterns **29** themselves be 30% or more on an area of a specified surface from a viewpoint of forming a properly tapered shape on the lower conductive material **3** without forming the undercut thereto while dissolving the upper conductive material **4** at a required rate.

Moreover, when the dummy conductive patterns **29** are arranged in the present invention, it is more preferable that the dummy conductive patterns **29** be formed between the end **30** of the pixel electrode **22** and each connection pads **25** and **27** so that the wiring density including the dummy conductive patterns **29** can be 30% or more on the area of a specified surface. In the present invention, the term "wiring density" refers to an area ratio of an area of portions where the signal lines, the scan lines, the drawing lines, and the dummy conductive patterns are formed on an area of a specified region where the dummy conductive patterns are formed.

FIG. **4** is a view showing another embodiment of the dummy conductive pattern **29** of the present invention. In the embodiment shown in FIG. **4**, the dummy conductive pattern **29** is disposed so that the wiring density thereof, which is specified at 30% or more, is further increased, thus reducing concentration of electric current to exposed portions of the upper conductive material to the etchant during the etching. As shown in FIG. **4**, the dummy conductive pattern **29** may have any shapes and any patterns. Moreover, any combination of a plural type of the dummy conductive patterns **29** can be used.

FIGS. **5**A, **5**B and **5**C are views showing an embodiment of a method of manufacturing the array substrate **10** for display of the present invention. With reference to FIG. **5**, description will be made for the method of manufacturing the array substrate **10** for display of the present invention, exemplifying a case where the thin film transistor **21** of a reverse stagger type is formed. First, as shown in FIG. **5**A, the lower conductive material **3** using aluminum and the upper conductive material **4** using molybdenum are deposited on the transparent or untransparent insulating substrate **1**, thus forming a film.

Next, as shown in FIG. **5**B, photoresist **31** is coated on the film. The photoresist is exposed and developed by use of a photo mask **32** provided with patterns for forming the dummy conductive patterns **29** in portions where the wiring density is lowered between the pixel electrodes and the connection pads, which are not particularly shown.

Subsequently, etching is performed by use of an etchant such as a solution of phosphoric acid, nitric acid, acetic acid and mixtures thereof, thus forming the wiring **2** and the dummy conductive patterns **29**. The dummy conductive patterns **29** are arranged in the portions where the wiring density is low. Thus, it is made possible to form wirings having good tapered shape as shown in FIG. **5**C even in regions where the conductive material such as molybdenum tends to be passivated. A taper angle can be set in a range of 20 degrees to 70 degrees by adjusting a composition of the etchant and etching conditions. It is more preferable to set the taper angle in a range of about 20 degrees to about 60 degrees.

Thereafter, in the present invention, gate insulating films, the gate electrodes, the source electrodes, the drain electrodes, the pixel electrodes and the like are formed, thus the array substrate **10** for display of the present invention is manufactured. In the present invention, the dummy conductive patterns **29** may be removed if necessary. Alternatively, the dummy conductive patterns **29** may be left as they are without being eliminated.

FIG. **6** is an electron microscope photograph showing a shape of the wiring **33** shown in FIG. **3**, which was obtained when the dummy conductive pattern **29** shown in FIG. **3** was provided and the etching was performed. In this case, molybdenum was used for the upper conductive material **4**, and aluminum was used for the lower conductive material **3**. The film thickness of molybdenum is about 50 nm, and wet etching is performed by use of an etchant of a mixed solution of phosphoric acid, nitric acid and acetic acid. As shown in FIG. **6**, a good tapered shape is formed even in a wiring portion where the undercut is formerly apt to occur by forming the dummy conductive pattern **29**.

FIG. **7** is a photograph showing a shape of the wiring **34** shown in FIG. **4**, which was obtained when the dummy conductive pattern **29** shown in FIG. **4** was formed and the etching was performed under the same conditions as those in FIG. **6**. As shown in FIG. **7**, even when the density of the dummy conductive pattern **29** is increased, a good tapered shape is obtained.

FIG. **8** is a graph plotting values of the taper angle of the formed wiring relative to values of the pattern density (area %) of the wiring including the portions of the dummy conductive patterns **29** on the substrate when the dummy conductive patterns **29** are arranged. As shown in FIG. **8**, the taper angle of the wiring obtained by the etching is reduced as the pattern density of the wiring is increased, and a more gentle taper is formed. Therefore, it is understood that the upper conductive material **4** can impart a sufficient selective ratio to the etching of the lower conductive material **3** by arranging the dummy conductive patterns **29**.

FIG. **9** is an electron microscope photograph showing, for comparison, a shape of wiring obtained when etching is performed by use of the array substrate **10** for display, which has the same pattern as those shown in FIGS. **3** and **4**, but without forming the dummy conductive patterns **29** at all. As shown in FIG. **9**, large undercut occurs in the wiring since the molybdenum used for the upper conductive material **4** is passivated, and only the etching for the aluminum as the lower conductive material **3** progresses.

FIG. **10** is an electron microscope photograph showing a cross section taken along a cutting plane line A—A of the wiring shown in FIG. **9**. As shown in FIG. **10**, the etching for the aluminum used for the lower conductive material **3** progresses more than that for the molybdenum used for the upper conductive material **4**, resulting in the occurrence of the great undercut.

The present invention can be applied not only to the thin film transistor of a reverse stagger type as described above but also to a thin film transistor of a top gate type including wiring formed of aluminum and any metal other than the aluminum, of which passivating current density is known.

Moreover, although the array device for display of the present invention can be applied to a liquid crystal display device using a transparent insulating substrate made of such as glass, the array device for display of the present invention can be also used as an organic or inorganic electroluminescence device, wherein an untransparent insulating substrate is used and an array for display is formed on the insulating substrate.

As described above, according to the present invention, it is made possible to provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of being etched at a sufficiently high etching rate and a sufficient selection ratio, and eliminating the under cut and the lowering of a yield in manufacturing due to the inconvenience such as an interlayer short circuit. Moreover, according to the present invention, it is made possible to provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of providing a large-sized and high-resolution display device.

Although the preferred embodiments of the present invention have been described in detail, it should be understood that various changes, substitutions and alternations can be made therein without departing from spirit and scope of the inventions as defined by the appended claims.

What is claimed is:

1. An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

2. The array substrate for display according to claim **1** wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

3. The array substrate for display according to claim **2** wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

4. The array substrate for display according to claim **2** wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

5. The array substrate for display according to claim **3** wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

6. The array substrate for display according to claim **5** wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

7. The array substrate for display according to claim **4** wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

8. The array substrate for display according to claim **5** wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

9. A meted for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array formed on the insulating substrate, each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

10. The method for forming an array substrate for display according to claim **9** wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

11. The method for forming an array substrate for display according to claim **10** wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.

12. The method for forming an array substrate for display according to claim **10** wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

13. The method for forming an array substrate for display according to claim **11** wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and allays thereof.

14. The method for forming an array substrate for display according to claim **13** wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

15. The method for forming an array substrate for display according to claim **12** wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

16. The method for forming an array substrate for display according to claim **13** wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

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